DX-70TH/EH

(HF&50MHz 100W Version)

Service Manual

CONTENTS

ALINCO, INC.

SPECIFICATIONS

1) General

Operating mode		J3E (LSB, USB), A1A (CW), F3E (FM)
Number of memory channels		100
Antenna impedance		50Ω unbalanced
Power requirement		13.8V DC ± 15% (11.7 to 15.8 V DC)
Grounding method		Negative ground
Current drain	Receive	1.0A max.
	Transmit	25A max.
Operating temperature		-10°C to +60°C
Frequency stability		± 10ppm (-10°C to +50°C)
Dimensions		178(w) x 58(h) x 228(d) mm (179 x 71x 268 mm for projections included)
Weight		Approx. 2.7kg

2) Transmitter

Transmit frequency coverage (e.g. U.S. Version)		160m band	1.8000 to 1.9999MHz
		80m band	3.5000 to 3.9999MHz
		40m band	7.0000 to 7.2999MHz
		30m band	10.1000 to 10.1499MHz
		20m band	14.0000 to 14.3499MHz
		17m band	18.0680 to 18.1679MHz
		15m band	21.0000 to 21.4499MHz
		12m band	24.8900 to 24.9899MHz
		10m band	28.0000 to 29.6999MHz
		6m band	50.0000 to 53.9999MHz
Power output	HF, 50MHz band	SSB, CW, FM	100W (high)
			Approx. 10W (low)
		AM	40W (high)
			Approx. 4W (low)
Modulation system		SSB	Balanced modulation
		AM	Low power modulation
		FM	Reactance modulation
Spurious emission		HF bands	Less than -50dB (-45dB in 10MHz band)
		50MHz band	Less than -60dB
Carrier suppression			More than 40dB
Sideband suppression			More than 50dB (at 1kHz)
Maximum FM deviation (default)		HF bands	± 2.5kHz
		50MHz band	± 5kHz
Microphone impedance			2kΩ

3) Receiver

Receiver circuitry			Double conversion superheterodyne
Receive frequency range			0.1500MHz to 30.0000MHz, 50.0000MHz to 54.0000MHz
Intermediate frequency			71.75MHz (1st), 455kHz (2nd)
Sensitivity	SSB, CW (S/N 10dB)	0.5 to 1.8MHz	0dB (1μV)
		1.8 to 30MHz	-12dB (0.25μV)
		50 to 54MHz	-16dB (0.15μV)
	AM (1kHz, 30% Mod, S/N 10dB)	0.5 to 1.8MHz	+20dB (10μV)
		1.8 to 30MHz	+6dB (2μV)
		50 to 54MHz	+6dB (2μV)
	FM (1kHz, 3.5kHz DEV SINAD 12dB)	28 to 30MHz	-6dB (0.5μV)
		50 to 54MHz	-10dB (0.3μV)
Selectivity	SSB, AM (Narrow)		2.4kHz/-6dB, 4.5kHz/-60dB
	SSB (Narrow), CW (Standard)		1.0kHz/-6dB, 3.0kHz/-60dB
	CW (Narrow)		500Hz/-6dB, 3.0kHz/-60dB
	AM (Standard), FM		9kHz/-6dB, 20kHz/-50dB
Spurious and image rejection ratio			More than 70dB
Audio output power			More than 2.0W (at 8Ω, 10% THD)
RIX/TXIT range			±1.4kHz

CIRCUIT DESCRIPTION

1. Receiving System

1) Filter Unit

a. Antenna Input

The electric charge on antenna is discharged by R501 or R507, and when the voltage exceeds about 300V, the gap in SA501 discharges thereby protecting the receive input circuit.
The input signal from antenna is passed through the HF/50MHz selecting relay RL503, the transmission/reception selecting relay RL502 and the attenuator relay RL514.
The LPF (consisting of L520, C545 and C546) filters out the followings: 2m band image receiving, passing through the First IF (71.75MHz), and leakage of the first local oscillating frequency (72~130MHz) to the antenna terminal.

b. 50MHz Antenna Input

The receiving signal from the antenna of 50MHz band is passed through the LPF and through the selecting relays RL503, RL514 and RL509, led to HPF.
The signal is amplified about 8dB in Q502. Because the space noise in 50MHz band is less than that in the HF band, its exclusive receiving preamplifier is expected to attain high sensitivity.
The receiving signal of 50MHz or HF is selected in RL509, then after passing through LPF consisting of L521, L522, C547, C548, C555, C556 and C557, the receiving signal is led to the Main unit.

2) Main Unit

a. Front End

The receiving signal output from Filter Unit is fed to Main unit through CN2.
HPF, consisting of L19, L20, C47, C48, C49, C50, C51 and C52, eliminates the strong radio signal of MW band of 1.6MHz or below. In case of receiving the signal of 1.6MHz or below, the sensitivity is controlled by the attenuator in R37 and BPF1, also the signal is separated into 1.6MHz, over or below.
5 BPF units consists of 9 filters. Each filter covers the following frequency range. The frequency of 2.5MHz or more consists of Chebyshëv BPF, and under 2.5MHz frequency band is LPF. Two BPF's are installed on the same unit. Not to be influenced so much, the distant frequency band BPF's are combined.

- 1.6MHz	BPF1	
1.6 - 2.5MHz	BPF2	1.8MHz
2.5 - 4.5MHz	BPF3	3.5MHz
4.5 - 7.5MHz	BPF4	7MHz
7.5 - 10.5MHz	BPF1	10MHz
10.5 - 14.5MHz	BPF2	14MHz
14.5 - 21.5MHz	BPF3	18, 21MHz
21.5 - 30MHz	BPF4	24, 28MHz
50 - 54MHz	BPF5	50MHz

Passing through BPF, the signal turns ON/OFF in the switching diode, D29 and D30. This preamplifier is the parallel grounded gate operation of Q9 and Q10 (2SK2171), so the unit can obtain a good performance at a high level input signal with low NF.
The wide range frequency from about 1MHz to 60MHz is amplified about 10dB. This 10dB preamplifier and 20dB attenuator in the Filter unit are combined, then by pressing RF gain switch on the front panel, one of four steps, -20, -10, 0, or +10dB is selected.
The LPF, consisting of L52, L53, L54, C103, C104, C105, and C106, prevents the following first receiving mixer from the local oscillation leaking, and also prevents the first IF and image of the spurious receiving.
The first receiving mixer consisting of Q10 and Q11 is the balanced mixer, in which the local oscillating signal is fed to the gate of 2SK2171.
The 3rd intercept point is about 20dBm, and local oscillator of about 2V P-P is fed to the gate. The receiving signal is converted into the first IF of 71.75MHz.
As the ratio of the spurious interference is decreased in 50MHz band mode, the trap of 71.75MHz consisting of L72 and C107 keeps the ratio of spurious interference 70dB or more in all band.

b. The First IF Amplifier Circuit

FL1: A and FL1: B are the crystal filters of 71.75MHz. By the combination of two filters, the unit has the characteristics of the band width of 15kHz or more/3dB and the value of guaranteed attenuation of 70dB or more. Here the image ratio is determined 70dB or more (approx. 80dB). The first IF amplifier circuit of Q12 is located between the crystal filters to prevent the loss in the front-end and mutual interference.
The first IF amplifier circuit Q12 decides the sensitivity after passing the mixer. AGC voltage is applied to the second gate.

c. The Second Mixer Circuit, The Second Amplifier Circuit

DBM (Double Balanced Mixer) consists of L14, D7 and L16. The signal is passed in the opposite direction while receiving or transmitting in this DBM. Approximately 0dBm is fed as the second local oscillating level, and the third IP is approximately 10dBm.
The receiving signal (71.75MHz) and the second local oscillating frequency (71.295MHz) is mixed, and unwanted signal is eliminated in LPF consisting of L17, L73 and C36, then the signal of 455kHz is generated. After passing through the switching diode D8, the signal is amplified in Q22. The source of Q22 is controlled by the output of the noise blanker circuit.

d. IF Filter

After passing through the transmission/reception switching diode D9, the signal is led to one of three ceramic filters of 455kHz. The selectivity is decided here except CW narrow.

SSB, AM-NARROW	FL3(CFJ455K5)	2.4kHz/-6dB	4.5kHz/-60dB
SSB-NARROW, CW	FL2(CFJ455K8)	1.0kHz/-6dB	3.0kHz/-60dB
FM, AM	FL4(CFW455G)	9kHz/-6dB	20kHz/-50dB

Each filter has 4 switching diodes (D3~D48) in front and rear to isolate the filter. The isolation is required the value of guaranteed attenuation of each filter (approx. 70dB) or more. The diode connected in parallel in front and rear of no used filter is

short and the diode connected in series is open. The combination of open and short is used to get the high isolation.
The modes, transmission/reception and wide/narrow of this filter are selected by Q36~Q46, D79, D80, D82, D83, D84.

e. The Second IF Amplifier Circuit

After passing through the filter, the signal is led to the transmission/reception switching diode D49, and amplified in Q23 and Q24, then buffered in Q25.
The AGC voltage is applied to the second gate of Q22, Q23 and Q24.
The output level of Q25 is fixed because the AGC voltage is added to the receiving signal.
This output signal is used for the demodulation in SSB, AM and CW modes and AGC detection.
In the FM mode, after passing through the transmission/reception switching diode of D49, a part of receiving signal is fed to IC7(MC3357) from C221, then it is IF-amplified and demodulated. C214 is connected in parallel to the feedback resister R182, and the resister is de-emphasized. Even in the FM mode, Q23, Q24 and Q25 are active, also AGC is operated.

f. Demodulation Circuit

In SSB and CW modes, the following local oscillating frequency is supplied from PLL unit to IC3 balanced mixer, then the signal is demodulated.
The receiving signal is fed to Pin1, and local oscillation Pin3, then picked up the demodulation output of approximately 100mV from Pin7.

USB	456.5kHz	+IF	SHIFT
LSB	453.5kHz	+IF	SHIFT
CWU	455.8kHz	+IF	SHIFT
CWL	454.2kHz	+IF	SHIFT

The output is led to the switching circuit of each mode, and to the CW audio filter.
In AM mode, the signal is detected in D51, then led to IC5.
In FM mode, the signal is demodulated and de-emphasized in above-mentioned IC7, then led to IC5.

g. CW Audio Filter

IC4 is the active filter, which consists of the combination of low-pass filter and high-pass filter in the operational amplifier. It has the band width of about 600Hz (-6dB) centering the frequency of about 800Hz.

h. AF, AGC Time Constant Selection

IC5 is the analogue multiplexer which has 2 circuits with 4 contact points, and switches the demodulation output in every mode and AGC time constant. The voltage combined in D55 and D56 is input to Pin9 and Pin10, then the output of IC3 (SSB, CW-W), the modulation output of FM/AM and CW audio filter output (CW-N) are selected. The voltage of 8V is applied to Pin6 (INHIBIT) when transmitting, and the modulation output is turned OFF unconditionally.

i. AF Amplifier

The voltage that can pass through the analogue switch of IC5 is very low. The voltage is amplified approximately 20dB in IC12: B to get higher AF input voltage to following IC13 (voltage controlled electronic volume). Also a part of this output is picked up and output to Pin6 of microphone as non-squelched audio output. This output is used as the terminal of packet, RTTY, SSTV, etc.

j. Electronic Volume, AF Amplifier

IC13 is the dual electronic volume controlled by the voltage.
The volume is controlled by the AF GAIN VR on the front panel. Pin5 is the control terminal. The value of the attenuation is the minimum when the control voltage is about 3.4V, and the value is 90dB or more at maximum when the control voltage is about 3.1V.
One of the circuits is for volume control of the demodulation sound, and the other for the volume control of the beep and sidetone. The beep and sidetone can be heard even if the volume is set to the minimum point and sound tone is related with AF GAIN VR.
The squelch circuit (IC14:A, Q14) controls Pin5. The output of IC14: A activates to close the squelch when transmitting, so Q14 is turned OFF in D85 to control the volume of the sidetone.
The receiving sound is fed to Pin6 and applied from Pin7. As for the beep and side tones, Pin2 is for input and Pin1 for output. These two outputs are combined with the input of LPF amplifier IC12:A. The high tone noise that is generated in IF amplifier is decreased by LPF amplifier.
The output of IC12: A is attenuated in R309 and R310 to get the same level with IC20, and also to decrease the noise. IC20 is the AF power amplifier which can get the output of 2W or more (THD 10%) at 8Ω load. The ripple filter consists of Q51 and C260.

k. AGC

The AGC voltage is supplied one stage to first IF amplifier and three stages to second IF amplifier. These IF amplifiers consist of 3SK131. AGC voltage is applied to the Gate2. The IF amplifiers are designed that the gain is changed linearly corresponding to the AGC voltage.
D53 and D54 are the rectifier, and Q26 is DC amplifier. D50, the anode is set to about 2V in R176, D110, D111 and R177. Usually AGC voltage is applied 2.4V. The strong signal rectifies D53 and D54 resulting in DC voltage. Q26 decreases the AGC voltage.
When AGC-FAST is selected in SSB/CW mode, C205 and C206 are connected between 5V and AGC line in parallel. The attack time of AGC is determined in R167 and C206, then the release time is determined in R168 and C206. The characteristics are "fast attack" and "slow release". In case of AGC-SLOW, the analogue switch IC6 is turned ON, then R175 and C287 are connected in parallel. The release time is lengthened because of C287. In case of AM, C206 is connected in parallel, then the attack time is delayed, which is the average type. D110 and D111 is the thermal compensation of D50.
In receiving AM, AGC is the average type not to follow the modulation.

l. S Meter, Squelch

The output of Pin1 and RF meter output are combined in the diode, then it is sent to the front CPU to display the meter. The output signal of Pin1 is fed to Pin6 of IC14:A. The voltage of Pin5 is determined by the squelch VR of front unit. Comparing with this voltage, the squelch is opened or closed.
While the check operation the CPU output decreases the voltage of squelch VR in front side to open the squelch forcedly. The squelch output controls IC13, at the same time it is provided to the front unit to light RX LED and led to CPU unit.

m. Noise Blanker Circuit

This circuit eliminates the pulse noise of a car, etc. Because the noise emitting time is short, in this duration the operation of receiver is stopped to prevent the unit from emitting a noise. The pulse noise is delayed when it is passed through the narrow band filter, and the emitting time becomes longer. It makes difficult to eliminate the noise, so it is necessary to eliminate the noise in the earlier stage.
A part of the second mixer output, whose band width is limited, is amplified in Q20, Q19, Q18, and Q16. The signal is detected in D33 and D34, and the AGC voltage is applied to Q19, Q18 and Q16.
The charge time constant of this AGC is determined by R82 and C128, and also the discharge constant is determined by R81+R82, C128. The voltage of AGC does not rise suddenly because of the charge constant, so that this voltage is not applied to almost all the short signals such as pulse noise, but is applied to the continuous signals such as receiving signal and amplifier gain is decreased.
While emitting the pulse noise, the AGC voltage does not follow the pulse noise, so the detected voltage is high, then Q15 is turned ON in that time.
On the contrary, as for the continuous signal, the detected voltage of D33 and D34 is fixed by AGC, so Q15 is turned OFF because of the emitter bias of R85 and R84.
Namely Q15 is turned ON only the time of the pulse noise, then Q21 is turned OFF. The source of IF amplifier of Q22 is biased through R98 and R102 so that the gain is decreased and the signal is blanked. When the emitter of Q15 is biased to high, the Noise Blanker is turned OFF.

2. Transmitter System

1) Main Unit

a. Microphone Amplifier

The input signal from microphone is amplified by the low noise amplifier Q56 through the mic gain VR1. It is possible to bias (8V) the microphone terminal with R388 for the microphone which needs the power supply. (solder bridge)
In SSB/AM mode, The gain of IC21 (approx. 15dB) is determined by R329 and R328.
In FM mode, R330 is connected to R320 in parallel by Q55, then the gain is increased approximately 34dB. Also the cut off frequency is risen, and the signal is pre-emphasized and operated as a limitter.
In the SSB/AM mode, C345 and R384 are conntected to the feedback circuit by Q63 when the speech compressor is turned ON. The gain is increased about 15dB, then IC21:B is operated as the limitter.
When the speech compressor is ON, the low frequency is cut by C345.
In FM mode, the gain is risen enough, so the speech compressor has no effect.
The output of Pin1 of IC21: B is attenuated in R326 and R325. The subaudible tone from PLL unit is applied through R325. (When the Tone is ON.)
IC21: A is LPF amplifier that is the Splutter filter in FM mode, and it is operated for speech compressor.
This signal is output to PLL unit as the FM modulation, and output to the balanced modulation of IC2.
The output to IC2 is muted by Q54 in CW/FM mode.

b. Balanced Mixer

IC2 is the balanced mixer, and the carrier is suppressed in SSB mode. To get more ratio of carrier suppression, the balance adjustment of VR3 and VR4 are applied.
The carrier is necessary in CW/FM/AM mode, so the input of Pin1 is made unbalanced by applying the DC voltage to obtain the carrier.
By applying the DC in AM/FM mode, or by keying in CW mode, the balance is broken to obtain the carrier wave. VR11 is used for the adjustment of carrier level.
In the AM mode, the DC and modulation is added simultaneously. In SSB mode, the modulation is added by R317. In AM mode, D93 is DC-biased and turned ON. Then the attenuator consisting of R317 and R393 limits the modulation.

c. IF Filter

After the output of IC2 increases the impedance in C177 and L77, it is passed through D49 and led into band limit IF filter. D52 is isolated highly by connecting to the output in parallel at receiving. In SSB mode, the output is DSB signal. (Double Side Band)
The filter is switched by the selection of above-mentioned diode switch. The signal is passed through the following filer in each mode.

SSB	FL3(CFJ455K5)	2.4kHz/-6dB	4.5kHz/-60dB
CW	FL2 (CFJ455K8)	1.0kHz/-6dB	3.0kHz/-60dB
FM, AM	FL4 (CFW455G)	9kHz/-6dB	20kHz/-50dB

SSB is obtained by eliminating one of side bands of DSB through the filter.

d. IF Amplifier, The Second Mixer

After passing through the filter, the signal is led to D37, Q7, and D6, and passed through the second mixer in the opposite direction of the receiving, then the signal of 71.75MHz is obtained. Q6 operates the CW keying.
The voltage of ALC is added to the second gate of Q7.
The local oscillating signal of 71.295MHz and unwanted signal are eliminated in FL1: A and FL5. The signal is amplified in Q5, passed through FL5, then led to the balanced mixer of Q3 and Q4.

e. The First Transmitting Mixer

This mixer is the balanced type, and the unwanted signals (IF and local oscillating signal) are decreased. The best operation is selected by biasing the second gate. To decrease the spurious, the signal is balanced in VR1.

f. Power Amplifier

Passing through the mixer, the transmitting signal which has the desired transmitting frequency is passed after switching the LPF for HF band or BPF for 50MHz band. The unwanted signal and especially the leak of local oscillating signal is decreased as less as possible.
The signal is amplified up to 0~3dBm in Q1. T notch filter consists of C1, C2 and L1. It is tuned to approximately 45MHz while using 50MHz band to decrease the spurious signal. Then the signal is supplied to PA unit.

2) PA Unit

a. Drive Amplifier

The signal input to PA unit is amplified up to approximately 100mW. The idling current of Q601 flows about 100mA during transmitting as A-class amplifier. The frequency characteristics are compensated by feedback, besides connecting the capacitor to emitter resistor in parallel.
The signal is amplified up to 5W in Q602 and Q603.
PA amplifier is the wide band range from 1.8MHz to 54MHz
The idling current flows 100mA (adjusted in VR601), and the amplifier is the push-pull type.
D601 is connected to Q602 and Q603 thermally, and the idling current is compensated for temperature.

b. Final Stage Power Amplifier

In the final stage amplifier circuit consisting of Q604 and Q605 (MRF255), the idling current of about 800mA is flowing. The gate bias is made by VR602, VR603.
The feedback circuit, consisting of L608, C625, R617 and R618, makes the gain flat in the wide range of 1.8MHz~54MHz.
The 100W output is led to filter unit.
The drain current of Q606 and Q607 is detected by using FB606 and L611. Then led to the main unit.

c. Fan Control

The heat of Q604 and Q605 is detected by the thermistor TH601, and the fan is controlled. While transmitting, the resistance value is decreased by the rising of the temperature, then the voltage of inverting input terminal of IC601A/B is decreased. Non-inverting input is applied with the settled voltage. When the temperature goes up to about 50°C or more and the compared inverting input voltage becomes lower than the non inverting input voltage, Q607 is turned ON by the output voltage of comparator, IC601: A. Then the fan starts turning at a low speed by the value of series resistor (R639).
When the temperature rises more and the voltage becomes much lower than the compared voltage IC601: B, Q608 is turned ON. Then R639 is turned OFF and the fan turns at a high speed according to the value of series resistor of R640 and decrease the compared voltage of IC601: A.
When the temperature goes up to about 100°C and the voltage is decreased further lower, IC601: A supplies again, then R639 and R640 are connected in parallel to turn the fan at a higher speed. Although ordinary PDWN is pulled up to 14V by R637, the power output is set to 50W because both cathode terminals of D608 become LOW when the fan turns at a high speed. Then the signal is sent to the main unit as the control signal for power down at high temperature.
As the compared voltage of IC601: B is decreased in D611 while receiving, IC601:B does not work if the temperature does not go up higher than it while transmitting. The temperature, at which the fan turns at a middle speed or more, is higher than it while transmitting. At high temperature, fan's turning speed comes down while receiving.

d. Protection Circuit

For the protection of the final power amplifier, the followings are equipped:
- SWR detection
- Protection against over current
- Power down circuit for the temperature detection

e. CW Keying Circuit

As the base voltage of main unit Q49 goes down to LOW by CW keying, the voltage is supplied to collector. This output controls all of the circuit operation by CW keying.
The collector output of Q49 is passed through D95, VR11 and D93, and the balance is broken by applying DC voltage to the balanced mixer to generate the carrier. VR11 determines the CW waveform of rise and fall by adjusting the carrier level in R285 and C248.
At the same time Q48 is turned ON to turn OFF Q6 for keying isolation. C244 makes the OFF time of Q6 longer not to influence the keying waveform.
The voltage is applied to IC17: B Pin5 in D95, and the output of Pin7 turns Q46 ON to set PTT line to LOW in D73, then the unit enters the transmitting mode. The capacitor (C246, C247) is connected between Pin5 of IC17: B and the ground.
The holding time of transmitting is determined according to the discharge time constant. BK1, BK2, and BK3 are the voltages for the setting of 3-bit break-in time constant. 8 stages voltage is obtained by the combination of the resistors R269, R270 and R271.
In the Full Break-in mode, all of BK1, BK2 and BK3 are set to LOW, in the Semi Break-in mode, one of BK1, BK2, or BK3 is applied the voltage.

When all of the breakers are applied the voltage, it is used as the shortest time constant.
When in the full break-in mode, all of the voltages of BK1, BK2 and BK3 are low level, and Q47 is turned OFF. Therefore only C246 is the very short discharge constant, it is the full break-in mode with short transmitting time. One of BK1, BK2 and BK3 is supplied the voltage, and Q47 is turned OFF, then connected to C247 and C246 in parallel. The discharge time constant is longer, and it is the semi break-in time constant.
There are 7 stages of the voltage in the semi break-in mode according to the output voltage of BK1, BK2 or BK3. This is applied to the compared voltage of IC17: B, then the discharge time constant is changed. Namely when the voltage is applied to all of BK1, BK2 and BK3, the time constant is the shortest.
When the break-in mode is set to AUTO, BK1 only is supplied, and the compared voltage of IC17:B is controlled by the output voltage of IC17: B.
In the AUTO mode the keying output is emitted by one-shot multivibrator consisting of IC18A and B whenever the key is pressed. Therefore the average value of the output voltage of IC18: A is in proportion to the average speed of keying. To obtain the average voltage in R281, C245, etc., integrate the voltage. Then this output is D/C amplified in IC17:A, and provided as the compared voltage of keying.
D97 is used for OFF in the AUTO mode. When the AUTO mode is in the LOW level, the voltage charged in C245 is short, then the operation in AUTO mode is stopped.
D107 and R360 are used to get up speed rising when the keying is started. D92 and R280 determine the discharge time constant. While receiving the time constant is prolonged.
The selection of transmission/reception follows the keying speed from 30 letters/minute to 200 letters/minute.
The transmitting mode is held between letters, and the unit returns to receiving mode between words.

f. Power Control, ALC Circuit

The forward wave voltage in proportion to the transmitting power obtained in filter unit is inverting-input to IC8:A, and inverting-amplified. Non-inverting input is applied the voltage, and the output voltage is shifted by the non-inverting input voltage.
ALC line is applied the voltage of about 2.7V beforehand, and the ALC voltage is supplied to the second gate of the amplifier.
When the forward wave voltage is detected, the output voltage of IC8: A is decreased. If it is about 3V or below, the ALC line voltage is decreased by D63.
VR7 is used for the adjustment of 100W. When the unit is switched to 50W by S1, Q27 is turned ON and VR5 is connected in parallel to decrease the voltage, then the unit is adjusted to 50W.
In AM mode, R195 is connected in parallel to decrease the voltage up to about 40W.
In the low power mode, R191 is connected in parallel by setting to LOW, and the voltage is decreased.
Q29 and VR8 are used for the adjustment to get the required power of about 10W in the matching operation of external automatic tuner. (The required power depends on the tuner.)
When the value of SWR is high, the reflected wave voltage turns Q28 ON to decrease the power. The unit is operated when the SWR is about 3 or more.

Compared with the forward wave detection power in HF band of 100 W, the forward wave voltage in 50MHz band of 10W is set to higher a little.
In SSB mode, "fast attack" is obtained by D63, and the release time of "slow attack" is obtained by C222 and R130. In AM mode C221 is connected in parallel by Q30, and the unit is operated in near the average value.

g. Over Current Protection Circuit

The final stage collector current which is detected in PA unit is differential-amplified in IC8: B. The output voltage is decreased according to the increase of the current. Then ALC line is fallen by D63 and the output power is decreased. The operational point is decided in VR6.

h. RF Meter Circuit, ALC Indication

The forward wave is amplified in IC9: A to obtain the meter output voltage.
The peak is held in D70, R223 and C223, and the meter swings smoothly.
Meter output voltage and S meter output voltage are switched in D71 and D86 automatically.
ALC voltage is inverting voltage amplified in IC9: B.
This output is applied to the base of Q31, then sent to front unit for the detection of transmission/reception and lighting the transmitting LED. The LED brightness is changed according to the ALC voltage.

i. Sidetone Circuit

The comparison frequency of the second local oscillator in PLL unit (65kHz~85kHz) is divided by 10 in IC714, then led to the main unit. In addition the frequency is divided by 10 in IC19 of the main unit to obtain the sidetone of 650Hz~850Hz. The comparison frequency of the second local oscillator is changed according to the CW offset setting. To relate with the sidetone, comparison frequency is about 100 times the CW offset. IC19 Pin2 is controlled by Q65 at CW keying. The time constant is delayed not to give the influence to waveform of the sidetone.
The following active filter Q50 makes the square wave to sine wave to obtain better sound. The rise/fall wave of the sidetone is generated by keying controlling the bias of base and emitter.

j. Tune Circuit

When using the external automatic antenna tuner, this circuit controls the matching start signal and the operation of the unit during tuner matching.
When the tune operation is started, the Tune voltage is supplied to operate the one-shot multivibrator in IC18: C, D. The voltage of about 8 V is applied to outside for a fixed time through Q52 as the start signal. In the other hand, Q53 supplies the tune voltage of sink output, it becomes LOW while tuning. (For the transceiver made by ICOM, KENWOOD).
As soon as the tuner receives the tune start signal, the tuner provides it as the tuning signal . (TKEY terminal)
CPU observes the TKEY terminal, and keeps the unit in TUNE mode indicating that the tuner is operating while it is in the LOW level. CPU releases the TUNE mode when TKEY terminal is in LOW for 20 seconds or more. In the Tune mode the unit transmits a signal in AM mode, the microphone output is muted, then the carrier is kept on outputting about 10W (adjustable).

k. Regulated Power Supply Circuit

IC11 is the 8V Regulated Power Supply Circuit. T8V that is necessary for transmitting is made in Q33, and R8V that is necessary for receiving is made in Q35.
IC10, Q32 and Q34 control the transmission/reception. When PTT line is connected to the ground through the microphone terminal or CW keying output (Q46), H level is supplied from IC10: A and it is led to CPU of front unit to detect the transmission/reception switching.
IC10: C delays the rise of receiving in R227, C224 and D62 and controls in Q32 and Q33.
While receiving, the current is flowing from 13.8V through R230 and D75, then the base voltage Q33 is approximately 8.7V, and the emitter output is just 8V.
While transmitting, the base voltage of Q33 is 0V because Q32 is turned ON, and R8V is not provided.
While transmitting R8V is short by D77, and it makes the charge voltage such as electrolytic capacitor discharge momentarily not to remain R8V.
As for Q35, as same as R8V the current is flowing from 13.8V through R230 and D75, then the base voltage of Q35 is approximately 8.7V and the emitter output is just 8V while receiving. While transmitting, the base voltage is 0V because Q34 is turned ON, and T8V is not provided.
While transmitting T8V is short by D77, and it makes the charge voltage such as electrolytic capacitor discharge momentarily not to remain T8V.
After delayed the transmitting rise time in IC10:B, the signal is inverted in IC18:D, then T8V is controlled in Q34.
When Pin8 IC10:A is supplied the voltage, the unit enters PTT lock mode without changing the output of Pin10 even if the PTT line is connected to the ground.

l. Mode Voltage, Function Control (BPF/ LPF Selector)

The enable terminals of IC15 and IC16 select the signal ENX or ENY by using IC24 and Q62.
The data from CPU (DAT2) consists of 16-bit serial data, two 8-bit shift resistors are connected in series.
IC22 and IC23 control the band selection, ON/OFF of preamplifier, ATT, power, TX mute function, etc. They are operated in Low level.
IC15 controls the Mode voltage, and IC16 controls filter, AGC, Break-in, PTT lock, and Noise blanker. The voltage of every mode (USB, LSB, AM, CW, CWU, CWL, FM, TUNE) turns ON Q41, Q42, Q43 and Q44 to supply 8V .

m. LPF

HF supplied from PA final stage eliminates harmonics through LPF of filter unit.
Input/Output of this filter is switched by the relay, and Input/Output of unused filter is short at the relay contact.
LPF control is used the BPF control voltage of the main unit.
Every LPF consists of Chebyshëv filter, and double or more harmonics are attenuated about 40dB or more.

L0	~ 2.5MHz	BB0, BB1	1.8MHz band
L1	2.5MHz~4.0MHz	BB2	3.5MHz band
L2	4.0MHz~7.5MHz	BB3	7MHz band
L3	7.5MHz~14.5MHz	BB4, BB5	10, 14MHz band
L4	14.5MHz~21.5MHz	BB6	18, 21MHz band
L5	21.5MHz~30.0MHz	BB7	24, 28MHz band

The transmitting signal, whose spurious is eliminated by passing through LPF, is led to power detection circuit and supplied to HF antenna terminal passing through the selection relay.

n. 50MHz Transmission/Reception Selector

50MHz band performs the transmission/reception selection by the relay RL503. It is supplied to antenna terminal of 50MHz through LPF consisting of L507, L508, C510, C511, C513, C517 and C518.
50MHz LPF consists of Chebyshev filter and double or more harmonics are attenuated 60dB or more.

o. Power Detection Circuit

A power detection circuit is equipped.
The harmonics are sometimes generated depending on the using diode in the detection circuit. LPF makes the standing wave, so the circuit is located before the LPF in 50MHz band whose spurious specification is severe, and after LPF in HF band.
L502 is 8 turns bifilar of toroidal core (twisted pairs of AWG). Therefore the both sides are 16 turns with center tap.
Piercing the center hole of the core means the same with 1 turn. So the transformer is 1:16.
Therefore R514 is applied the voltage (forward wave voltage) according to the output voltage, and R515 is applied the voltage (reflected wave) according to the reflected power. The output power and reflection detect the power to control the power in the main unit.

p. Dial Rotating Detection

The pulse generated by the rotation of the main dial is eliminated the chattering in IC1001: A, B. IC1001: A and B are the Schmitt triggers by the feedback from the output.
The rise and fall of each output is differentiated in IC1002:A, C, so the pulse number is doubled. Then it is 4 times the pulse number because of synthesizing in IC1001: C.
To find the rotation direction, it is detected in IC1002: B and IC1003 and fed to CPU. As S1002 generates 50 pulse at 1 rotation, what is input to CPU is 200 pulse/rotation, and 5kHz/rotation in 25Hz step.
The main dial rotates very fast and generates so many pulses. The pulse is divided in IC1004, and the pulse number is stored as the 6-bit binary digit by each dividing output. At a high speed rotation the frequency is forwarded by counting the pulse number stored in IC1004, then the process is finished, the pulse number stored in IC1004 is reset by the output from CPU.
The dial rotation pulse is charged in D1016, R1022 and C1010, and the average voltage according to the speed is obtained. When the dial rotation speed is fast, the frequency step per pulse is four times that at normal speed.

3) Front Unit

a. Power Switch

When SW1001 is pressed, Q1001 is turned ON, then the contact of RL602 in PA unit is turned ON to supply the voltage of 13.8V to the front unit. Once the CPU starts operation, the output from PCONT of CPU turns Q1006 ON to hold ON the relay of RL602.
When SW1001 is kept pressing while the power is ON, the signal is detected in PSDET, and the Q1006 is turned OFF to cut OFF the power supply.

b. Power Supply

IC1007 is the regulated power supply of 5V which has the output for CPU reset.
IC1006 is the regulated power supply of 8V which generates the required voltage for IF shift and volume control.
When the power supply is cut OFF, the output of regulated power supply of 8V is increased first, and it is detected in D1018 and IC1002:D, then sent to CPU. In CPU the data is stored in the EEPROM of IC1005 before the output of regulated power supply of 5V is decreased and the unit is reset. D1019 and C1002 are used to hold the output voltage of 5V by keeping the input voltage of 5V regulated power supply as long as possible.

c. Dimmer Circuit

The regulated power supply of about 10.5V consists of Q1003, Q1004 and Q1005.
Q1003 supplies about 10.5V when the DIMM output from CPU is 5V.
In CPU unit, DIMM is the pulse output, and it switches ON/OFF of the output of about 10.5V.
At full lighting the output from CPU is fixed to 5V. In "LP4" mode the duty is 80% and in "LP 3 " mode the duty is 60%. In this way the brightness is changed by the duty in Q1003.
Q1003 is supplied the current by turning ON/OFF. At the maximum the brightness is the lightest, and the duty is decreased according to the dimmer, then the power dissipation is decreased. The dimmer can be operated by the small transistor.
The maximum brightness is 10.5V, and it is set to under the regulation voltage (6.3V x 2) to prolong the life of the lamp. The rush current when the lamp is turned ON is in pulse mode to decrease the load on the lamp.

d. LCD

The indication such as frequency that is required the speed is performed by the CPU itself, and the other indications are performed by the LCD driver of IC1009.
The LCD indication employs the frame frequency of about 128Hz, 1/2 DUTY and 1/2 bias.

e. Others

X1001 is the ceramic resonator of 8MHz selected not to enter the amateur band in the harmonics relations.
When the power is ON, the voltage is supplied from Y2 and Y3, to detect whether it is connected to the outputs DB0~DB6 or not, then the destination is determined.
The currents in Y0 and Y1, and between DB~DB6 are scanned to detect which switch on the front panel is pressed.
The both sides of RIT VR are applied 5V, and the location of VR is detected by the voltage of A/D input terminal.
In the Receiving frequency monitor Q1019 is turned ON by the MONI output from CPU, the squelch setting voltage programmed by turning the knob on the front panel is decreased forcedly. Then the squelch is open forcedly without any relation with VR position.
The output from the main unit (RTXC) lights the LED according to the change of the ALC voltage. The output cannot be supplied as it is, so it is changed to ON/OFF signal in Q1009.
Q1011 is the squelch output from the main unit, and it lights RX LED.

4) PLL Unit

Summary

The followings are performed in PLL unit:

- The generation of carrier signal
- The generation of the first and second local oscillating signal
- The generation of sidetone CTCSS
- Adding the FM modulation
- Making the power supply of 5V

Details

(1) There are 3 kinds of power supply as follows:
- The voltage of 13V passed through the switch
- The voltage of 8V made in the MAIN unit
- The voltage of 5V made in the PLL unit

Power supply depending on the MODE comes from the main unit.
(2) First the reference signal of 30MHz is generated in X701 and Q701 according to the constant of TC701 and L702.
(3) Secondly the signal of 9.420MHz +/- 1.5kHz is generated by the voltage of D706 in X702, Q721 and Q722.
(4) Thirdly the signal of 9.875MHz +/- 1.5kHz is generated according to the constant of TC702-TC704, C807, C809, C810, C811 and C812 in Q725 and Q724.
(5) The frequency of 9.875MHz is changed according to the MODE, transmission/reception.

[Transmission/Reception of LSB]
CN701 Pin21 (LSB) is applied the voltage of 8V and the signal is passed through D714, then results in the frequency of 9.8735MHz according to the constant of TC702 and C812. Also (LSB) 8V is passed through D718, and the voltage is applied to Q723 to emit the carrier signal.

[Transmission/Reception of USB]
CN701 Pin26 (USB) is applied the voltage of 8V and the signal is passed through D711, then results in the frequency of 9.8765MHz according to the constant of TC704 and C807. Also (LSB) 8V is passed through D717, and the voltage is applied to Q723 to emit the carrier signal.

[Reception of AM/FM/TUNE]
CN701 Pin20 (FM) or CN701 Pin22 (AT) is added the voltage of 8V and in the FM mode the signal is passed through D708, then results in the frequency of 9.875MHz according to the constant of TC703 and C811. Q723 has no voltage,

and carrier signal is never emitted.

[Transmission of AM/TUNE]
CN701 Pin22(AT) is applied 8V and results in the frequency of 9.875MHz according to the constant of TC703, C811.
The voltage of 8V from CN701 Pin23 (T8V) is passed through D718 to add the voltage to Q723, then the carrier signal is emitted.

[Transmission of FM]
CN701 Pin20 (FM) and CN701 Pin23 (T8V) are added the voltage of 8V , the Q729 and Q733 are turned ON. 8V voltage of CN701 Pin20 (FM) is passed through D708, Q733 and D714, then results in the frequency of 9.8735MHz according to the constant of TC702 and C812. Here FM is passed through AT and R814 to turn ON C811, however, as Q733 is also turned ON, Q727 is turned ON and C811 is shorted.
The voltage of 8V from CN701 Pin23 (T8V) is passed through D718, and led to Q723 to emit the carrier signal.
The voltage of 8V from Q733 turns ON the analogue switch of IC715.
The modulation signal is passed through R798, IC715, R796 and C801, and it is FM-modulated in VCO2.

[The Transmission of CWU/CWL]
CN701 Pin24 (CWU) or CN701 Pin25 (CWL) is supplied the voltage of 8V, then it is passed through D716, D732, Q716 (because Q729 is ON) and R814, then results in the frequency of 9.875MHz according to the constant of TC703 and C811.
Although here CWU tries to turn C810 ON or CWL tries to turn C809 ON, it can not be done through D715 because Q729 is also turned ON.

[The Reception of CWU]
CN701 Pin24 (CWU) is supplied the voltage of 8V, passed through D712, then resulting in the frequency of 9.8758MHz of frequency according to the constant of TC703 and C810. Also the voltage of 8V from CN701 Pin24 (CWL) is passed through D716 and D717 to the Q723, then the carrier signal is emitted.

[The Reception of CWL]
CN701 Pin25 (CWU) is supplied the voltage of 8V, passed through D712, then resulting in the frequency of 9.8742MHz of frequency according to the constant of TC703 and C809. Also the voltage of 8V from CN701 Pin25 (CWL) is passed through D716 and D717 to the Q723, then the carrier signal is emitted.

(6) The frequency of 9.42MHz can be changed only while receiving by the IF shift volume on the front panel.

The voltage supplied to CN701 Pin14 (SHV) is changed by the IF shift volume, and the capacitance of D706 is also changed, then 9.42MHz is changed. The center frequency of the IF shift volume is determined by VR702.
While transmitting Q715 is turned ON by T8V to eliminate the influence by SHV and VR 701, then the frequency is decided only by VR701.

In USB CN701 Pin26 (USB) and CN701 Pin15 (TONS) are supplied the voltage of 8V. As in UT mode TONS becomes the sink, Q735 is turned OFF and USB is supplied 0V , then Q730 is turned ON and a terminal of R767 is connected to the ground to decrease the voltage of D706, beside the frequency of 9.42MHz is decreased about 300Hz less while receiving and about 100Hz less while transmitting than the value in USB mode.

In the same manner, in LSB mode the voltages of CN701 Pin21 (LSB) and CN701 Pin15 (TONS) are 8V. As in LT mode TONS becomes the sink, Q735 is turned OFF and D729 is supplied the voltage by R767. Then voltage of D706 is increased. Beside the frequency of 9.42Hz is increased about 300Hz more while receiving and about 100Hz more while transmitting than the value in LSB mode.

(7) The Emission of 455kHz Carrier Signal
The above-mentioned 9.875MHz signal is input to Mixer IC712 Pin6, and 9.42MHz signal is input to IC712 Pin8. The difference frequency of 455kHz is output from IC712 Pin3 and sent to the MAIN unit from J701 after amplified in Q723. The Output level is approximately -5dB.

(Frequency Relations depending on the Mode)

USB(TX RX)		9.8765MHz - 9.42MHz (**)	= 456.5kHz (**)
LSB(TX RX)	FM(TX)	9.8735MHz - 9.42MHz (**)	= 453.5kHz (**)
CWU CWL AM TUNE (TX)		9.8750MHz - 9.42MHz	= 455.0kHz (*)
CWU(RX)		9.8758MHz - 9.42MHz (*)	= 455. 8kHz(*)
CWL(RX)		9.8742MHz - 9.42MHz (*)	= 454. 2kHz (*)
UT(RX)		9.8765MHz - 9.4197MHz (*)	= 456.8kHz (*)
LT(RX)		9.8735MHz - 9.4203MHz (*)	= 453.2kHz (*)
UT(TX)		9.8765MHz - 9.4199MHz	= 456.6kHz
LT(TX)		9.8735MHz - 9.4201MHz	= 453.4kHz

AM FM (RX) does not output
(**): While receiving IF Shift Operation (+/- 1.5kHz)
(*): IF Shift Operation (+/- 1.5kHz)

(8) The Second Local Oscillating Signal
In VCO2 unit, after the frequency of 71.295MHz is oscillated in Q941 and amplified in Q949, Q944 and Q945, the signal of approximately 3dB is supplied to MAIN unit through J702 as the second local oscillating signal.
The signal for PLL loop is supplied from Q942 to PLL unit.
The signal of 71.295MHz is fed to Mixer IC711 Pin7 and the signal of 9.42MHz is fed to Pin3, so that the deference frequency of 61.875MHz output from Pin6 only is picked up by Q711, L712 and L711, and fed to PLL IC707, then locked at 61.875MHz.
Therefore, by rotating the IF shift volume, 9.42MHz, and also 71.295MHz are changed.
The frequency of 30MHz is fed to IC707 through Pin1, and it is divided to get the following frequency as the reference frequency, and also the frequency of 61.875MHz is divided to get the reference frequency, then these two frequencies are compared.
The reference frequency changes according to the CW sidetone frequency.

When the sidetone frequency is 650Hz, the reference frequency is 64.655kHz.
When the sidetone frequency is 750Hz, the reference frequency is 75.000kHz.
When the sidetone frequency is 850Hz, the reference frequency is 85.227kHz.

(9) The First Local Oscillating Signal

In the HF mode, the frequency oscillated in VCO3 is amplified in Q710 and Q714, and passed through the switching diode D725 and D726, then band-pass filter and RL701. The signal of approximately 3dB is led to the MAIN unit from J703.

3 VCO's are built in VCO3, and it is oscillated under following frequency conditions:

150kHz~under 10.5MHz:

The VCO is oscillated within 71.90~82.25MHz by D961, TC961 and Q961.

10.5kHz~under 21.5MHz:

The VCO is oscillated within 82.25~93.25MHz by D963, TC962 and Q963.

21.5kHz~under 30.0MHz:

The VCO is oscillated within 93.25~101.75MHz by D965, TC963 and Q965.

These 3 VOC's are selected by the serial data of DAT2, CK2 and ENB from CPU. 8 signals from IC716 are reduced up to 3 signals, then VCO is selected by the switches of VCO3, Q962, Q964 and Q966.

When the frequency is 50MHz, in VCO3 the oscillated frequency within 76.75~80.75MHz by D961, TC961 and Q961 are synthesized with the frequency of 45MHz by the DBM (Double Balanced Mixer) in L729, L730 and D730, then the frequency within 121.75~125.75MHz is generated. It is passed through RL701 by the band-pass filters of L732, L733, L734 and L735 and Amplifier of Q731 and Q716, then the signal of approximately 3dB is output to J703.

The frequency of 45MHz is generated as follows: The reference signal of 30MHz is amplified in Q719 and fed to IC701 Pin3, then one half of the signal is supplied from Pin5. 3 times frequency of the signal only is passed through the filter L720, L721 and L722, and fed to the center tap of L729, then led to DBM.

The frequency loop of VCO3 is locked as follows: VCO3 oscillating frequency is passed through Q712 and input to the mixer IC709 Pin6, also the signal of 70.65~70.75MHz (25Hz step) is fed to IC709 Pin8. Then the signal of 1.1~31.1MHz passed through the amplifier Q713 and led to PLL IC702 Pin8 as the difference signal.

This frequency is locked by the following procedure.

1.1MHz is added to the digit number of 100kHz or more of the operation frequency, and divided to obtain 100kHz. Then the frequency is locked after comparing with the reference frequency 100kHz. See the examples as shown below.

Operation Frequency: 1MHz

—> PLL The frequency fed to IC702 Pin8: 2.1MHz

Operation Frequency: 29MHz

—> PLL The frequency fed to IC702 Pin8: 30.1MHz

Therefore, as the reference frequency of IC702, the reference frequency of 30MHz is divided up to 100kHz inside the unit.

In IC702, the operation frequency of 100kHz or more only is controlled.

In 50MHz band, CN701 Pin1 (50M) is sink, Q732 collector is supplied the voltage of 8V. The power supply of Q731, Q716 is turned ON. Q709 and D730 are turned ON. Q709, RL701, D724 and D724 are turned ON, then D730 is ON and Q724 is OFF.

The deviation while transmitting is 5kHz/DEV, and 2.5kHz/DEV while HF/FM transmitting.

In the HF mode, Q717 is ON, and D725 and D726 are turned ON, then D735 is ON. IC710 Pin4 is supplied about 0.7V so that the operation of IC710 is stopped.

When the unlock signal is emitted from every Pin7 in PLL IC IC702, IC703 and IC707, the voltage of 8V is supplied from the collector in Q728, and Q718 is turned ON so that Q714 is turned OFF, then the level of J703 is decreased about 30dB or more.

(10) 25Hz Step 70.65~70.75MHz

In VCO1 Unit, to generate 25Hz step of the first local oscillating, Q931 is used to oscillate the frequency of 155MHz~175MHz, the signal is passed through Q932 and divided by 20 in IC704, and supplied through Q933. Then the signal is divided by 10 in IC705, and the frequency of 775~875kHz (25Hz step) is fed to the mixer IC701. Therefore, the operation frequency of 100kHz digit or below can be operated in 25Hz step.

Also the frequency is input to PLL unit IC703 Pin8 through Q931 for the PLL loop. PLL IC divides the frequency of 155.000~174.995MHz to get 5kHz, and it is compared with the reference frequency of 5kHz to make the loop.

Indication of the operation frequency of 100kHz digit or below	Oscillating frequency
.0000(00)	155.000MHz
.5000(00)	165.000MHz
.9999(75)	174.995MHz

*The number in ( ) is the frequency of no indication.

The reference frequency of 30MHz is divided to get 5kHz (25Hz x 200), and used as the reference frequency in IC703. Because the signal of 9.875MHz is input to IC701 Pin8, the sum of the frequencies, 10.65~10.75MHz is supplied from IC703 Pin2, and passed through the ceramic filter of 10.7MHz, then fed to IC706 Pin6.

As the double harmonics of reference frequency of 30MHz are generated in Q708, L710 and L709, and they are fed to IC706 Pin8. The sum of the frequency of 70.65~70.75MHz is supplied from IC703 Pin3, passed through the band-pass filter of L706, L707 and L708, and fed to IC709 Pin8. Then the signal is ncluded in a part of the loop of the first local oscillating signal.

(11) CTCSS for only FM transmission

In Tone unit, T type controls the frequency with the DIP Switch SW901 Pin3 - 8, then it is oscillated between 67~251Hz, amplified in Q901 and passed through CN704-1, then led to the MAIN unit from CN701 Pin16.

In this circuit, ON operation is performed when TONS is the sink and IC901 Pin4 is 0V, and FM is supplied 8V and tone unit power supply is ON.

The tone level is controlled with the DIP switch SW901 Pin1 and Pin2 to adjust the level.

(12) FM TX deviation

Default is ±2.5kHz deviation on 29MHz and ±5kHz deviation on 51MHz.

a) Short-circuiting collector and emitter of Q734 will make both bands ±2.5kHz.

b) Short-circuiting the base and emitter of Q734 (and collector and emitter open) will make both bands ±5kHz.

Short-circuiting both (a) and (b) will result in the same effect as (a).

5) Terminal function of CPU

No.	Use1	Use2	Use3	Pin Name	Remarks	I/O	Description	L	H
2			AVss	GND		-			
3				GND		-			
4			X2	XTAL, LOSC		-			
5			X1	XTAL		-			
6			Vss	GND		-			
7			OSC1	XTAL		-			
8			OSC2	XTAL		-			
9			/RES	/RST		I			
10			MDO	5V?		I			
11	P20	IRQ4	ADTRG	DCK	DIAL CLOCK	I	Main dial rotation detection and pulse number	Rise edge detection	
12	P21		UD	PCONT	POWER ON	O	Power control output	Power OFF	Power ON
13	P22			PSDET	POWER DET	I	Condition detection when power switch is turned ON.	During power OFF	During power ON
14	P23			TKEY	TUNE KEY	I	Detection of working external antenna tuner	At work	Waiting
15	P24			UNLK	PLL UNLOCK	I	PLL unlock detection	Unlock	Lock
16	P25			MCK	EEPROM CK	O	Clock for data transmission/reception to EEPROM		
17	P26			MDAT	EEPROM DATA	I/O	Data Transmission/Reception to EEPROM		
18	P27			EXTIN	EXT IN	I	External EEPROM transmission acceptance	EEPROM	Acceptance
19	P30		SCK1	CK1	SERIAL1 CK	O	HPL, LPL data transmission clock		
20	P31		SI1	DAT1	SERIAL1 DATA	O	HPL, LPL data transmission		
21	P32		SO1	ENH	HPLL ENABLE	O	HPL data transmission enable		Enable
22	P33		SCK2	ENL	LPLL ENABLE	O	LPL data transmission enable		Enable
23	P34		SI2	CK2	SERIAL2 CK	O	MODE, BPF, etc. transmission clock		
24	P35		SO2	DAT2	SERIAL2 DATA	O	MODE, BPF, etc. data transmission		
25	P36		STRB	ENA	SERIAL SELECT	O	MODE, BPF, etc. data enable selection		Enable 1
26	P37		CS	ENB	SERIAL SELECT	O	MODE, BPF, etc. data enable selection		Enable 2
27			Vss	GND		-			
28			V3			-			
29			V2			-			
30			V1			-			
31			Vcc	5V		-			
32	PA3	COM4		COM4		O	LCD COMMON		
33	PA2	COM3		COM4		O	LCD COMMON		
34	PA1	COM2		COM3		O	LCD COMMON		
35	PA0	COM1		COM3		O	LCD COMMON		
36	P50	SEG1	WKP0	DB0		I	SW, initial setting detection		Detection
37	P51	SEG2	WKP1	DB1		I	SW, initial setting detection		Detection
38	P52	SEG3	WKP2	DB2		I	SW, initial setting detection		Detection
39	P53	SEG4	WKP3	DB3		I	SW, initial setting detection		Detection
40	P54	SEG5	WKP4	DB4		I	SW, initial setting detection		Detection
41	P55	SEG6	WKP5	DB5		I	SW, initial setting detection		Detection
42	P56	SEG7	WKP6	DB6		I	SW, initial setting detection		Detection
43	P57	SEG8	WKP7			O			Detection
44	P60	SEG9		Y0		O	Panel SW for ON detection		At detecting
45	P61	SEG10		Y1		O	Panel SW for ON detection		At detecting
46	P62	SEG11		Y2		O	Output for initial condition setting detection		
47	P63	SEG12		Y3		O	Output for initial condition setting detection		
48	P64	SEG13		GND		O			
49	P65	SEG14		LCDEN		O	LCD driver enable		
50	P66	SEG15		LCDCK		O	LCD driver clock		
51	P67	SEG16		LCDATA		O	LCD driver data		

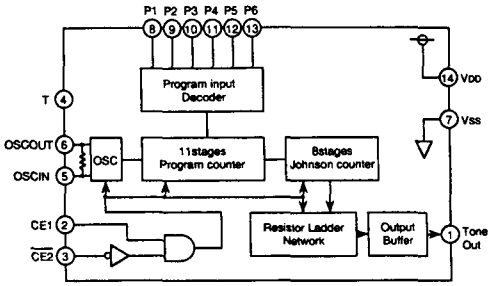
No.	Use1	Use2	Use3	Pin Name	Remarks	I/O	Description	L	H
52	P70	SEG17		SEG17		O	Output to LCD Segment		
53	P71	SEG18		SEG18		O	Output to LCD Segment		
54	P72	SEG19		SEG19		O	Output to LCD Segment		
55	P73	SEG20		SEG20		O	Output to LCD Segment		
56	P74	SEG21		SEG21		O	Output to LCD Segment		
57	P75	SEG22		SEG22		O	Output to LCD Segment		
58	P76	SEG23		SEG23		O	Output to LCD Segment		
59	P77	SEG24		SEG24		O	Output to LCD Segment		
60	P80	SEG25		SEG25		O	Output to LCD Segment		
61	P81	SEG26		SEG26		O	Output to LCD Segment		
62	P82	SEG27		SEG27		O	Output to LCD Segment		
63	P83	SEG28		SEG28		O	Output to LCD Segment		
64	P84	SEG29		SEG29		O	Output to LCD Segment		
65	P85	SEG30		SEG30		O	Output to LCD Segment		
66	P86	SEG31		SEG31		O	Output to LCD Segment		
67	P87	SEG32		SEG32		O	Output to LCD Segment		
68	P90	SEG33		SEG33		O	Output to LCD Segment		
69	P91	SEG34		SEG34		O	Output to LCD Segment		
70	P92	SEG35		SEG35		O	Output to LCD Segment		
71	P93	SEG36		SEG36		O	Output to LCD Segment		
72	P94	SEG37	M	SEG37		O	Output to LCD Segment		
73	P95	SEG38	D0	SEG38		O	Output to LCD Segment		
74	P96	SEG39	CL2	SEG39		O	Output to LCD Segment		
75	P97	SEG40	CL1	SEG40		O	Output to LCD Segment		
76			Vcc	5V		-			
77	P10		TMOW	MONI		O	Open the squelch forcedly (monitor)		Squelch open forcedly
78	P11		TMOFL	LIT		O	The command to put out the light forcedly and flashing to LCD driver	Put out the light forcedly	During lighting
79	P12		TMOFH	BEEP		O	Beep sound output	Pulse output	
80	P13		TMIG	SQS		I	Squelch open/close condition detection	Squelch close	Squelch open
81	P14		PWM	DIMM	DIMMER	O	LCD dimmer control	Duty control of pulse output	
82	P15	IRQ1	TMIB	TXS		I	Transmission condition detection	Transmission	Reception
83	P16	IRQ2	TMIC	SUBA		I	MF dial rotation detection		
84	P17	IRQ3	TMIF	SUBB		I	MF dial rotation detection		
85	P40		SCK3	DRST	COUNT RESET	O	Dial pulse count reset	During counting	Reset
86	P41		RXD	GND		I			
87	P42		TXD	GND		I			
88	P43	IRQ0		POWDN	POWER DOWN	I	Power OFF detection	Power OFF	Power OK
89			AVcc	5V		-			
90	PB0	AN0		DQ1		I	Dial clock 1/2		
91	PB1	AN1		DQ2		I	Dial clock 1/4		
92	PB2	AN2		DQ3		I	Dial clock 1/8		
93	PB3	AN3		DQ4		I	Dial clock 1/16		
94	PB4	AN4		DQ5		I	Dial clock 1/32		
95	PB5	AN5		DQ6		I	Dial clock 1/64		
96	PB6	AN6		DQ		I	Dial up rotation		Up
97	PB7	AN7		/DQ		I	Dial down rotation		Down
98	PC0	AN8		DSDET		A/D	Dial speed detection	The voltage according to the speed of rotation.	
99	PC1	AN9		RIT		A/D	RIT VR position detection	0~5V	
100	PC2	AN10		U/D		A/D	Mic UP/DOWN detection	2~3V down	0~2V up
1	PC3	AN11		SRF		A/D	S & RF Meter voltage input	0~5V	

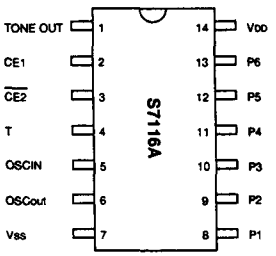
SEMICONDUCTOR DATA

1) S7116A (XA0052)

Tone Generator

Block Diagram



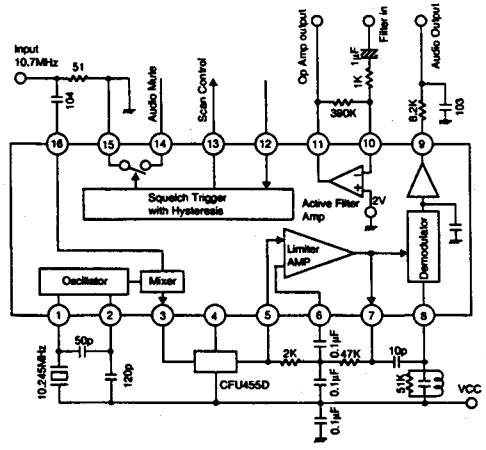


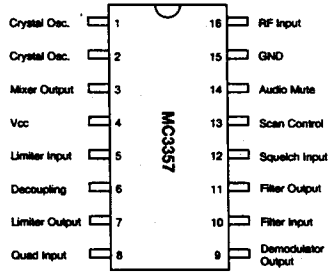
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	VDD		3.0	-	10	V
Supply current	IDDO	VDD=5.0V, CE1=VDD, $\overline{CE2}$=Vss, CG=CD=10pF	-	0.4	1.0	mA
Stand by current	IDDS	VDD=5.0V, input: open, RL=50kΩ	-	20	60	μA
Tone output level	VOT	VDD=5.0V, RL=50kΩ	240	340	440	mV rms

Freq.	P1	P2	P3	P4	P5	P6	Freq.	P1	P2	P3	P4	P5	P6
67.0	1						186.2		1	1	1	1	
71.9		1					192.8	1	1	1	1	1	
74.4	1	1					203.5						1
77.0			1				210.7	1					1
79.7	1		1				218.1		1				1
82.5		1	1				225.7	1	1				1
85.4	1	1	1				233.6			1			1
88.5				1			241.8	1		1			1
91.5	1			1			250.3		1	1			1
94.8		1		1			500	1	1	1			1
97.4	1	1		1			600				1		1
100.0			1	1			700	1			1		1
103.5	1		1	1			800		1		1		1
107.2		1	1	1			900	1	1		1		1
110.9	1	1	1	1			1000			1	1		1
114.8					1		1600	1		1	1		1
118.8	1				1		1700		1	1	1		1
123.0		1			1		1750	1	1	1	1		1
127.3	1	1			1		1800					1	1
131.8			1		1		1300	1				1	1
136.5	1		1		1		2000		1			1	1
141.3		1	1		1		2200	1	1			1	1
146.2	1	1	1		1		2975			1		1	1
151.4				1	1		2550	1		1		1	1
156.7	1			1	1		2295		1	1		1	1
162.2		1		1	1		2125	1	1	1		1	1
167.9	1	1		1	1		1275				1	1	1
173.8			1	1	1		1445	1			1	1	1
179.9	1		1	1	1								

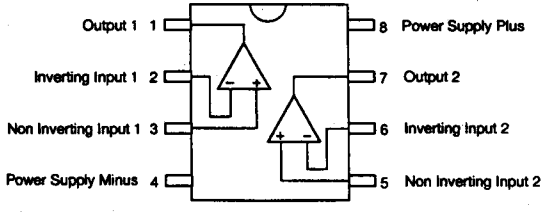
2) MC3357 (XA0063)
Low Power FM IF

Vcc=6V
F=10.7MHz
Icc 3mA
Limit 5μV -3dB
Vo 350mV Dev=+/-3KHz

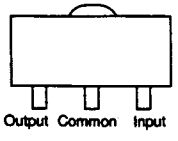




3) M5218FP (XA0068)
Dual Low Noise
Operational Amplifiers

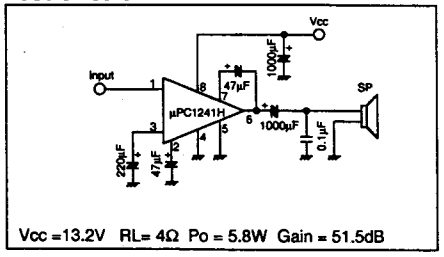


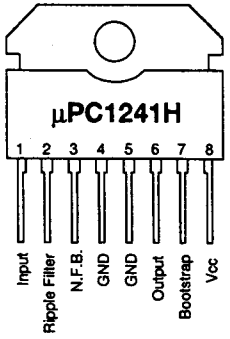
4) NJM78L08UA (XA0075)
8V Voltage Regulator



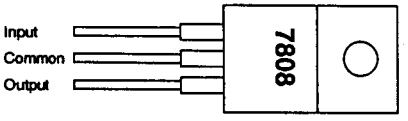
5) μPC1241H (XA0079)
Audio Power Amplifiers

Test Circuit



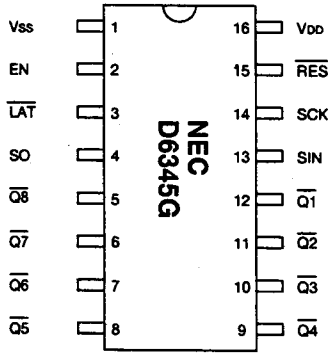


6) MC7808CT (XA0082)
8V Voltage Regulator

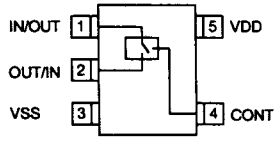


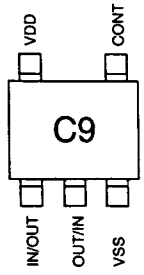
7) μPD6345GS (XA0114)
8bit Serial in Parallel Out Driver

No.	Pin Name	Description
1	GND	GND terminal
2	EN	Enable terminal
3	$\overline{LAT}$	Latch terminal
4	SO	Serial data output terminal
5-12	$\overline{Q8}$-Q1	Data output terminal
13	SIN	Serial data input terminal
14	SCK	Serial clock input terminal
15	$\overline{RES}$	Reset input terminal
16	VDD	Power supply terminal



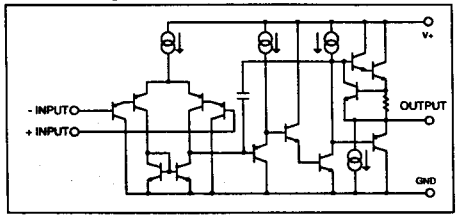
8) TC4S66F (XA0115)
Bilateral Switch

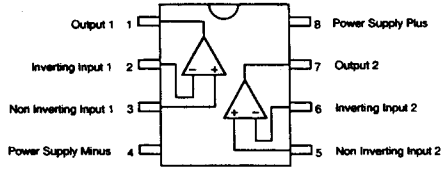




9) NJM2904M (XA0224)
Dual Operational Amplifiers

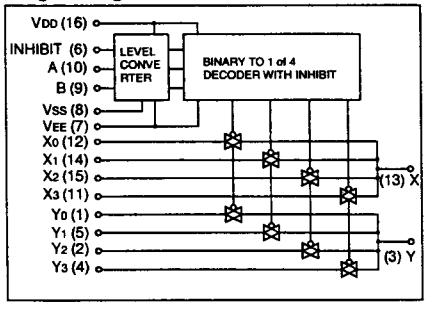
Block Diagram

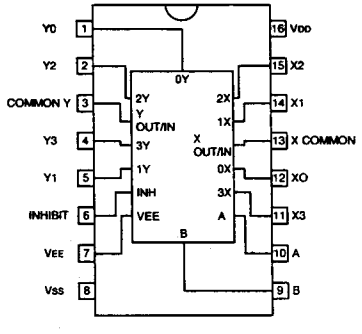




10) BU4052BF (XA0236)
Analog Multiplexer/Demultiplexer

Logic Diagram





Truth Table

INHIBIT	A	B	ON SWITCH
L	L	L	X0 Y0
L	H	L	X1 Y1
L	L	H	X2 Y2
L	H	H	X3 Y3
H	X	X	NONE

X: Don't Care

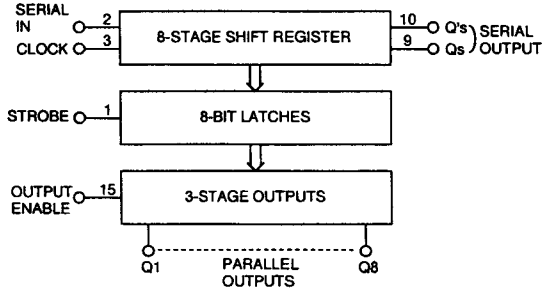
11) BU4094BF (XA0246)
8-Stage Shift Register

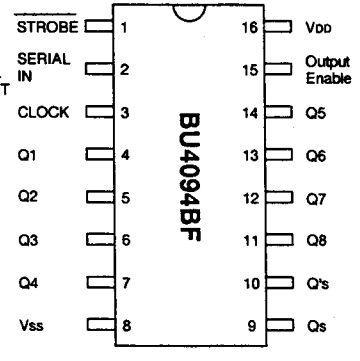
Truth Table

Clock	Output enable	Strobe	Data	Parallel outputs Q1	Parallel outputs Qn	Serial outputs Qs	Serial outputs Q's
↑	L	X	X	Z	Z	Q7	No Chg.
↓	L	X	X	Z	Z	No Chg.	Qs
↑	H	L	X	No Chg.	No Chg.	Q7	No Chg.
↑	H	H	L	L	Qn-1	Q7	No Chg.
↑	H	H	H	H	Qn-1	Q7	No Chg.
↓	H	X	X	No Chg.	No Chg.	No Chg.	Qs

Z=High Impedance
X=Don't Care

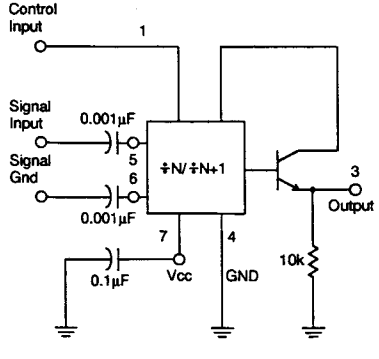
Block Diagram





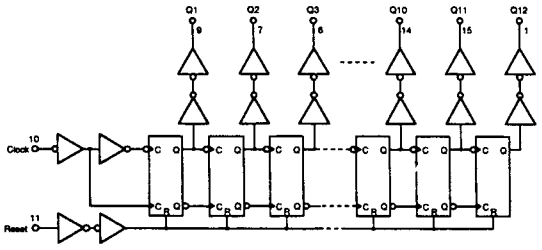
12) MC12019D (XA0292)
Two-Modulus Prescaler

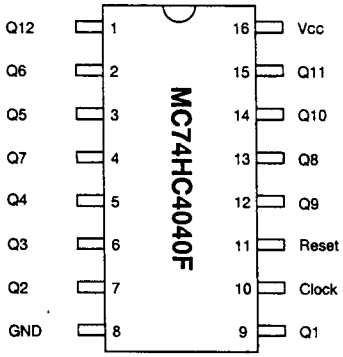
Block Diagram



Characteristics	Symbol	Min.	Typ	Max	Unit
Toggle frequency (Sine wave input)	fmax fmin	225 -	- -	- 20	MHz
Supply current	Icc	-	-	7.5	mA
Control input High (1/20)	VIH	2.0	-	-	V
Control input Low (1/21)	VIL	-	-	0.8	V
Output voltage swing	Vout	600	-	1200	mVpp
Input voltage sensitivity	Vin	200	-	800	mVpp
PLL response time	tPLL	-	-	tout-70	ns

13) MC74HC4040F (XA0293)
12-Stage Binary Ripple Counter

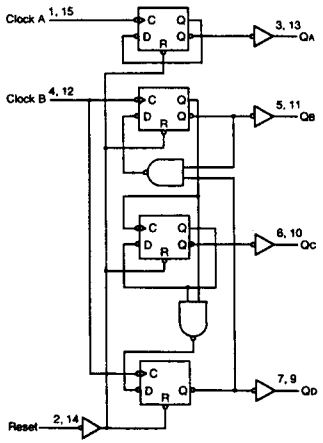


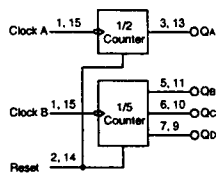


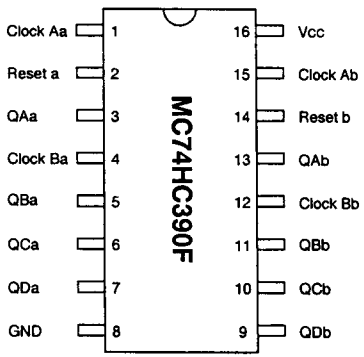
Truth Table

Clock	Reset	Output State
↑	L	No Change
↓	L	Advance to next stage
X	H	All outputs are low

14) MC74HC390F (XA0294)
Dual 4-Stage Binary Ripple Counter 1/2 and 1/5 Sections



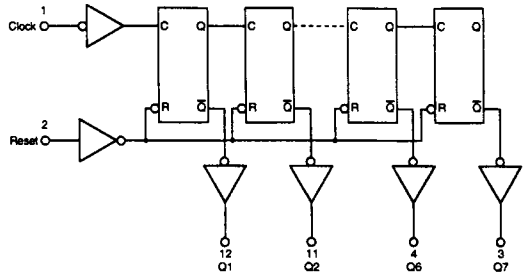


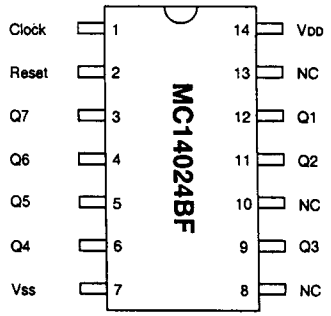


Truth Table

Clock		Reset	Action
A	B		
X	X	H	Reset 1/2 and 1/5
↓	X	L	Increment 1/2
X	↓	L	Increment 1/5

15) MC14024BF (XA0295)
7-Stage Binary Counter





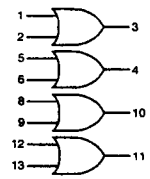
Truth Table

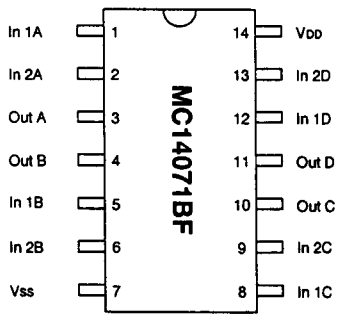
Clock	Clear	Output State
Don't care	H	All Output="L"
↑	L	No Charge
↓	L	Advance to next stage

16) MC14071BF (XA0296)
Quad 2-Input OR Gate

Truth Table

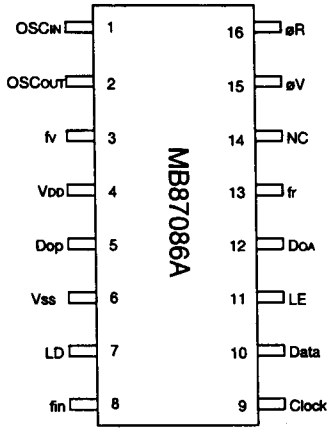
Input		Output
A	B	X
L	L	L
L	H	H
H	L	H
H	H	H

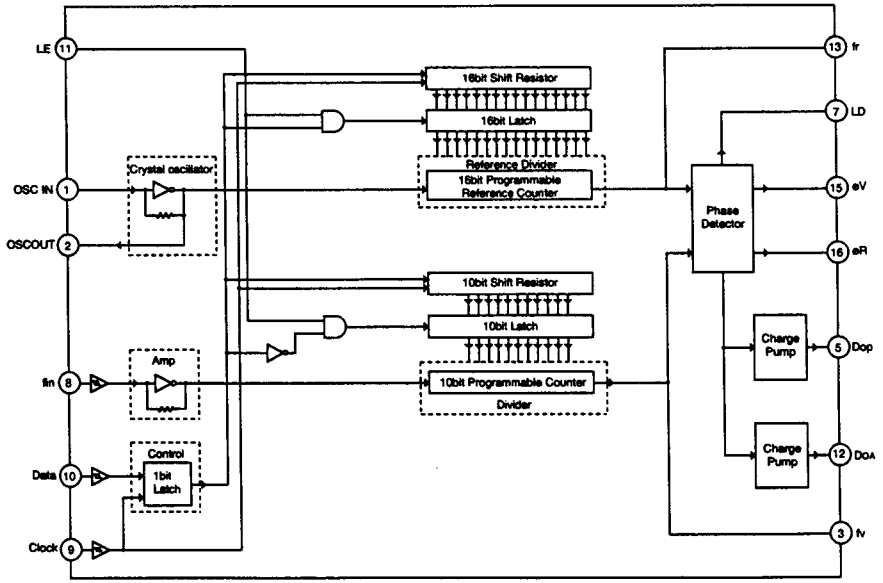




17) MB87086A (XA0297)
PLL Frequency Synthesizer

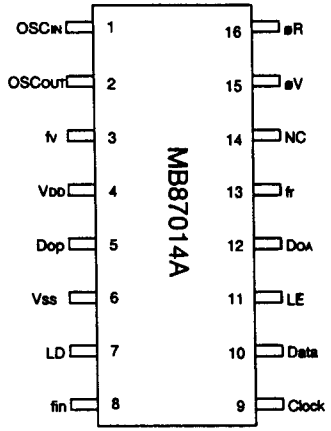
No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Crystal connection terminal
2	OSC_{OUT}	O	Crystal connection terminal
3	fv	O	Phase comparator input monitor terminal Comparator divider output terminal
4	V_{DD}	-	Power supply
5	Dop	O	Passive LPF connection terminal fr>fv: Drive mode, Dop="H" fr=fv: High impedance fr<fv: Sink mode, Dop="L"
6	Vss	-	GND terminal
7	LD	O	Phase detector output terminal Lock="H", Unlock=negative pulse
8	fin	I	Comparator divider input terminal
9	Clock	I	Serial clock input terminal
10	Data	I	Serial data input terminal
11	LE	I	Load enable input terminal
12	D_{OA}	O	Active LPF connection terminal fr>fv: Drive mode, D_{OA}="L" fr=fv: High impedance fr<fv: Sink mode, D_{OA}="H"
13	fr	O	Phase comparator input monitor terminal Reference divider output terminal
14	NC	-	No connection
15	øV	O	Differential LPF connection terminal fr>fv: øV="H", øR="L" fr=fv: øV="H", øR="H" fr<fv: øV="L", øR="H"
16	øR	O	

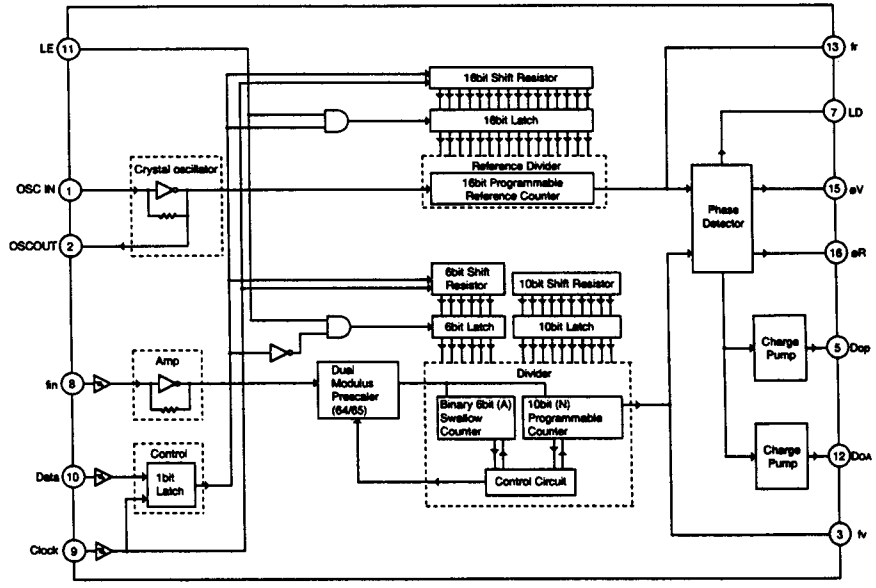




18) MB87014A (XA0298)
PLL Frequency Synthesizer

No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Crystal connection terminal
2	OSC_{OUT}	O	Crystal connection terminal
3	fv	O	Phase comparator input monitor terminal Comparator divider output terminal
4	V_{DD}	-	Power supply
5	Dop	O	Passive LPF connection terminal fr>fv: Drive mode, Dop="H" fr=fv: High impedance fr<fv: Sink mode, Dop="L"
6	Vss	-	GND terminal
7	LD	O	Phase detector output terminal Lock="H", Unlock=negative pulse
8	fin	I	Prescaler input terminal
9	Clock	I	Serial clock input terminal
10	Data	I	Serial data input terminal
11	LE	I	Load enable input terminal
12	D_{OA}	O	Active LPF connection terminal fr>fv: Sink mode, D_{OA}="L" fr=fv: High impedance fr<fv: Drive mode, D_{OA}="H"
13	fr	O	Phase comparator input monitor terminal Reference divider output terminal
14	NC	-	No connection
15	øV	O	Differential LPF connection terminal fr>fv: øV="H", øR="L" fr=fv: øV="H", øR="H" fr<fv: øV="L", øR="H"
16	øR	O	

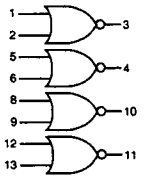


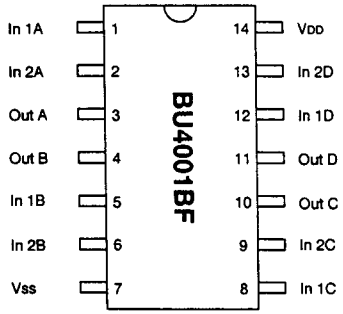


19) MC4001BF (XA0299)
Quad 2-Input NOR Gate

Truth Table

Input		Output
A	B	X
L	L	H
L	H	L
H	L	L
H	H	L

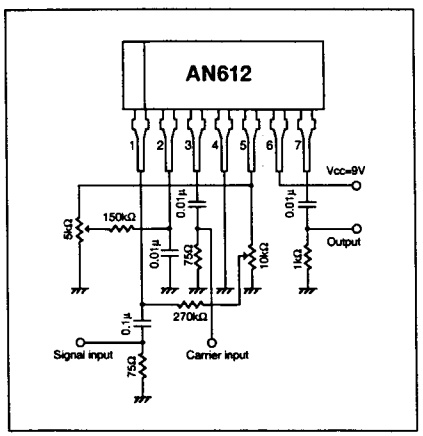


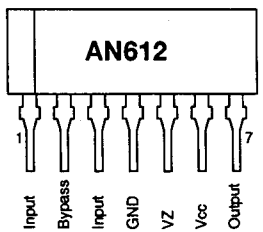


20) AN612 (XA0300)
Balanced Modulator Circuit

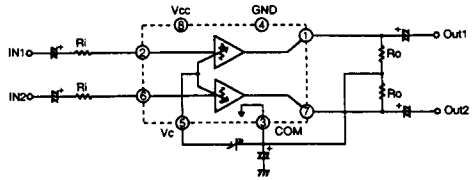
Parameter	Symbol	Condition	Ratings	Unit
Max. supply voltage	Vcc		14.4	V
Supply current	Icc		15	mA
Power dissipation	PD		220	mW
Total current	Itot	V6=12.0V	9.5	mA
Zener voltage	V5-4		6.15	V
Signal input terminal voltage	V1-4		3.1	V
Carrier input terminal voltage	V3-4		3.4	V
Output terminal voltage	V7-4		8.6	V
Output voltage (BM AC)	Vo(BM)	V6=9.0V	-3	dBm
Carrier suppression	SC		50	dB

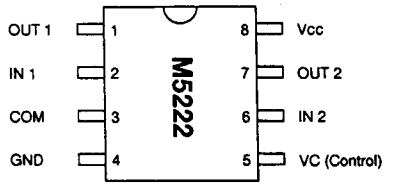
Test Circuit





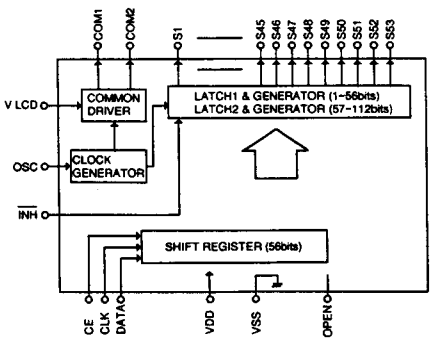
21) M5222FP (XA0385)
Low Voltage Dual VCA

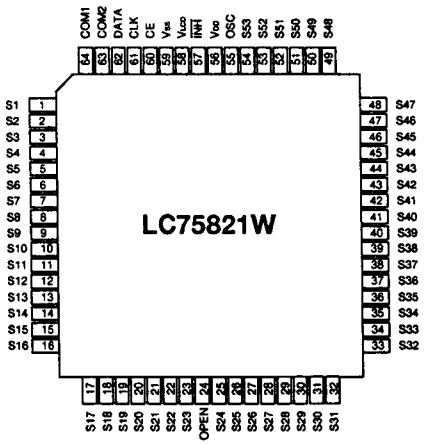




Parameter	Symbol	Condition	Vcc	Min	Typ	Max	Unit
Supply current	Icc	Vi=0, Vc=0	3V	2.5	3.6	5.5	mA
Max. input voltage	ViM1	f=1kHz, Vc=0, THD=1%, RI=10kΩ, RO=20kΩ	3V	0.7	1.0	-	Vrms
	ViM2	f=1kHz, Vc=0, THD=1%, RI=50kΩ, RO=100kΩ	9V	2.3	3.4	-	Vrms
Max. attenuation level	ATT_M	Vc=-270mV, RI=10kΩ, RO=20kΩ	3V	80	90	-	dB
Noise output voltage	V_{NO1}	Vc=0 (ATT=-1.4dB) RI=10kΩ, RO=20kΩ, BW=20Hz~20kHz	3V	-	30	60	μVrms
Noise output voltage	V_{NO2}	Vc=-40dB RI=10kΩ, RO=20kΩ, BW=20Hz~20kHz	3V	-	5	-	μVrms

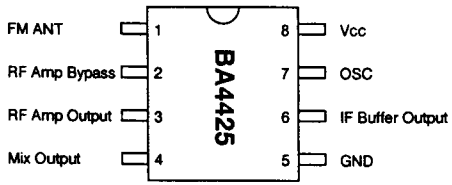
22) LC75821W (XA0303)
LCD Driver





Pin Name	Description
S1~S53	Segment output terminal
COM1, 2	Common output terminal
V LCD	LCD Bias voltage setting terminal
OSC	Oscillator terminal
CE, CLK, DATA	Serial data transmission terminal
VSS, VDD	Power supply terminal
$\overline{INH}$	Display turn off input terminal $\overline{INH}$="L" Vss, turn off (S1~S53, COM1,2="L") $\overline{INH}$="H" Vdd, turn on
OPEN	No connection

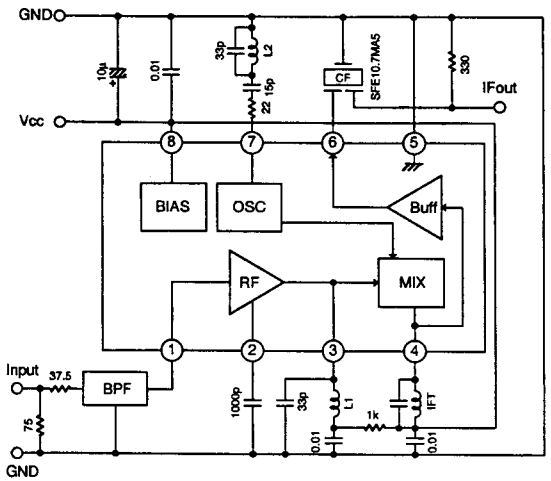
23) BA4425F (XA0304)
FM Front End IC



Vcc=4V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current	Io	No signal	2.6	4.5	7.2	mA
Saturated output voltage	Vo	fd=98MHz, 80dBμV	30	50	72	mV rms
Local oscillator voltage	Vosc	fosc=108MHz	200	400	630	mV rms
Conversion gain	Gvc	fd=98MHz, 55dBμV	31	36	42	dB
Local oscillator stop voltage	OSC STOP		-	-	1.2	V

Test Circuit

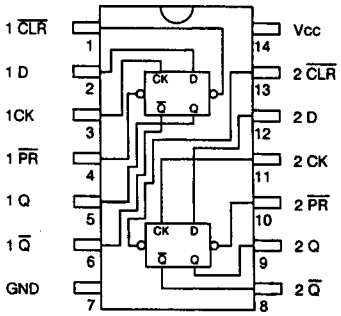


24) TC74AC74F (XA0305)
Dual D-Type Flip Flop

Truth Table

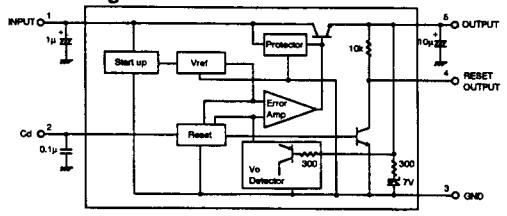
INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	-
H	H	L	↑	L	H	-
H	H	H	↑	H	L	-
H	H	X	↓	Qn	$\overline{Qn}$	NO CHARGE

X=Don't Care

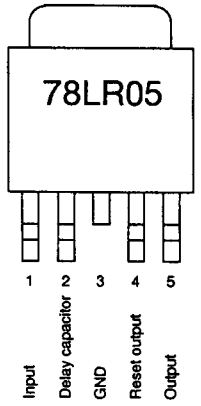


25) L78LR05B (XA0338)
Voltage Regulator

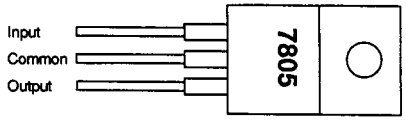
Block Diagram



Parameter	Symbol	Ratings	Unit
Input voltage	Vin	7.5~20	V
Output current	Iout	1~150	mA
Output voltage	Vout	5.0	V



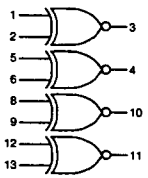
26) MCT7805 (XA0346)
5V Voltage Regulator

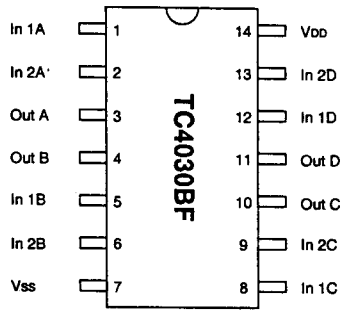


27) TC4030BF (XA0347)
Quad Exclusive-OR Gate

Truth Table

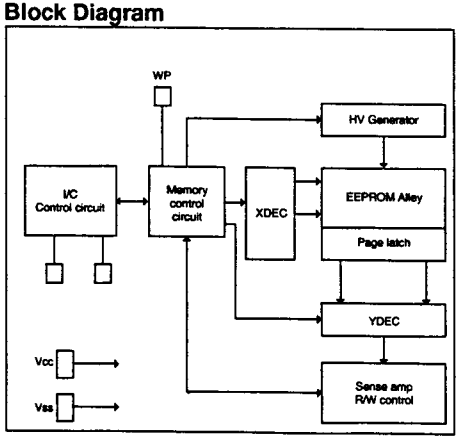
Input		Output
A	B	X
L	L	L
L	H	H
H	L	H
H	H	L

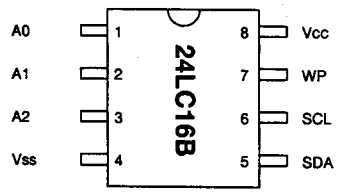




28) 24LC16B (XA0351)
16K bits CMOS Serial EEPROM

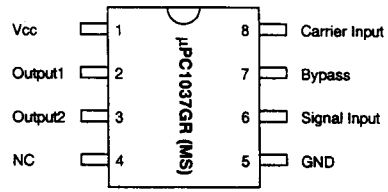
Block Diagram





Pin Name	Description
Vss	GND terminal
SDA	Serial address/data I/O
SCL	Serial clock
WP	Write protect
Vcc	+2.5V~5.5V power supply
A0, A1, A2	No connection

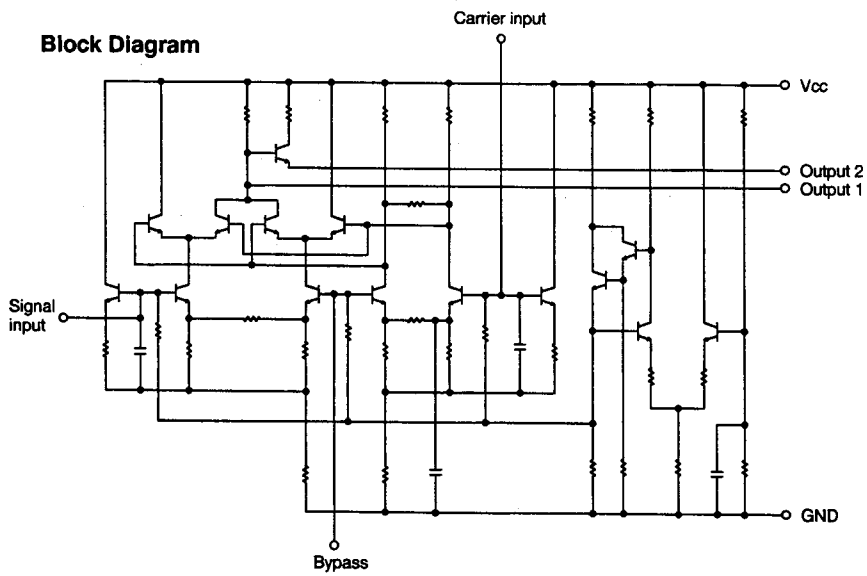
29) µPC1037GR (XA0379)
Double Balanced Modulator



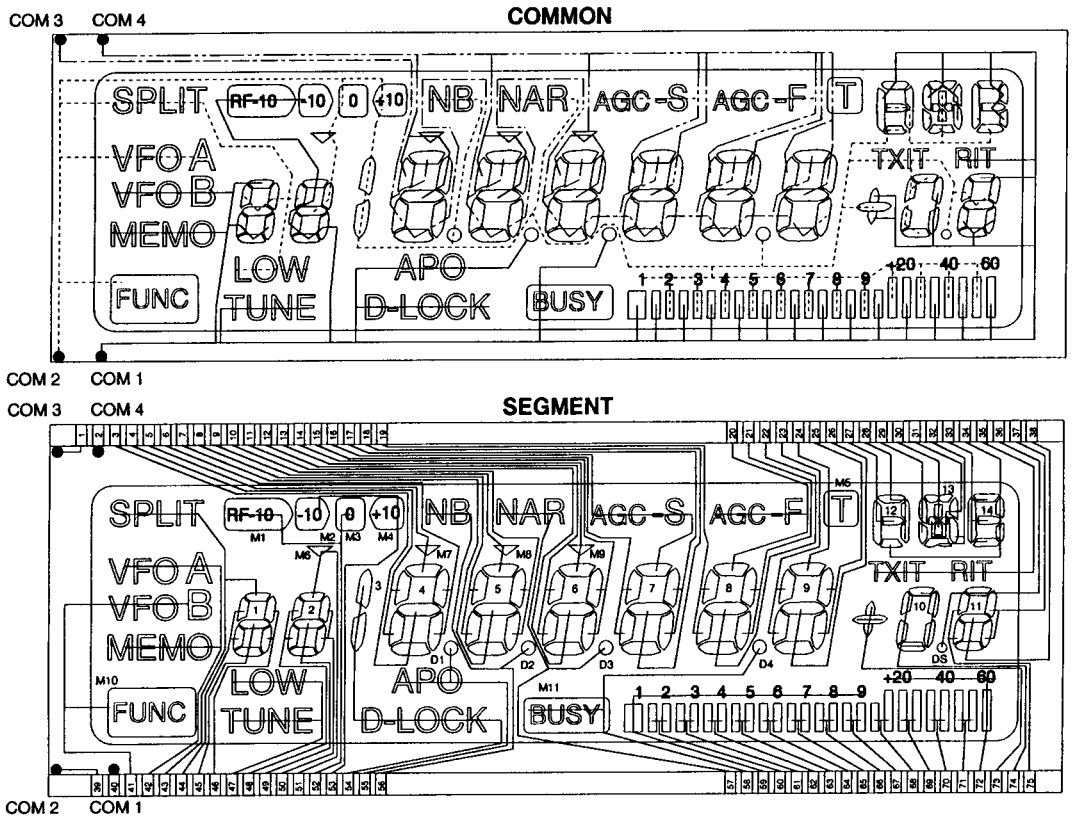
Vcc=6.0V

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Circuit current	Icc	No signal	-	12	16	mA
Conversion gain	Gc	Signal: 70mV r.m.s. 1.75MHz	-2	0	+2	dB
Signal leakage	Ls	Carrier: 100mV r.m.s. 28.25MHz	-	-40	-20	dB
Carrier leakage	Lc	Output: 30MHz	-	-32	-20	dB
Inter modulated distortion	IMD	Signal 1: 42.5mV r.m.s. 1.75MHz Signal 2: 42.5mV r.m.s. 2.00MHz Carrier: 100mV r.m.s. 28.25MHz Output: 29.75MHz	-	-45	-35	dB
Signal input impedance	Zsi		-	500//9	-	Ω//pF
Carrier input impedance	Zci		-	1.0//9	-	kΩ//pF
Output impedance	Zol	Output 1	-	350//7	-	Ω//pF

Block Diagram

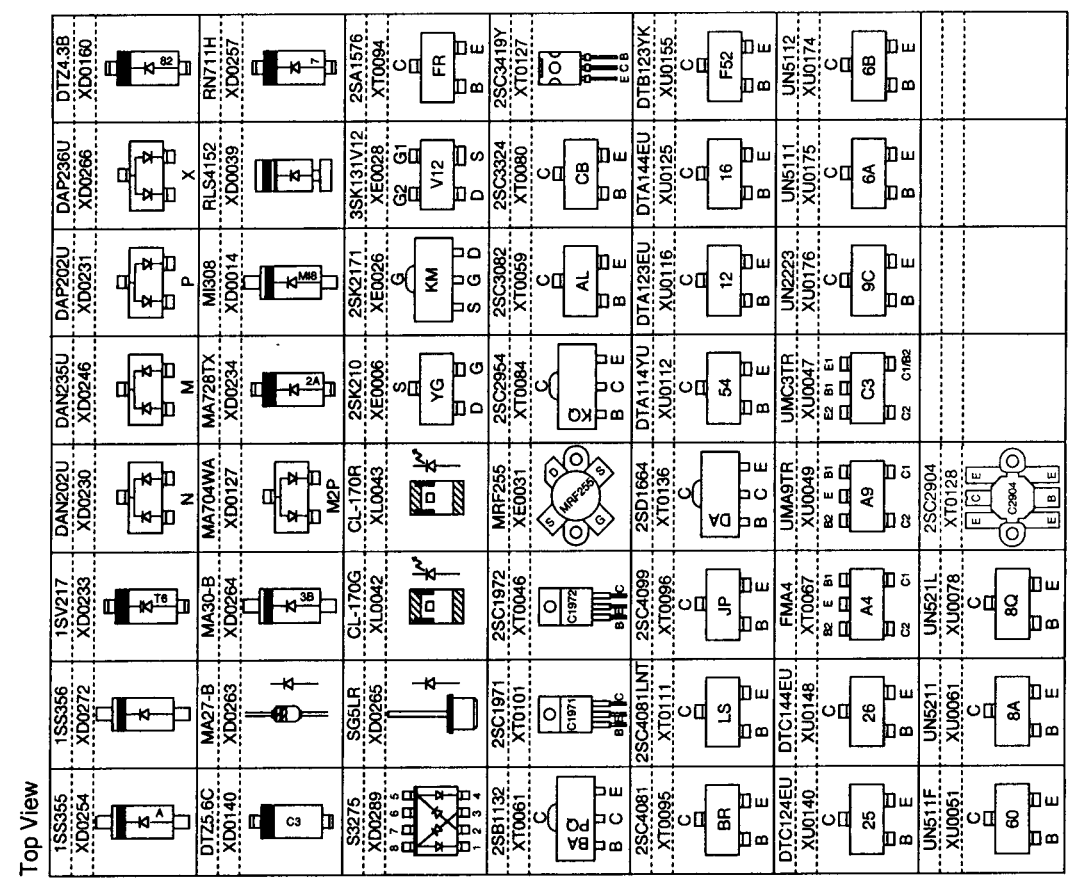


31) LCD Connection



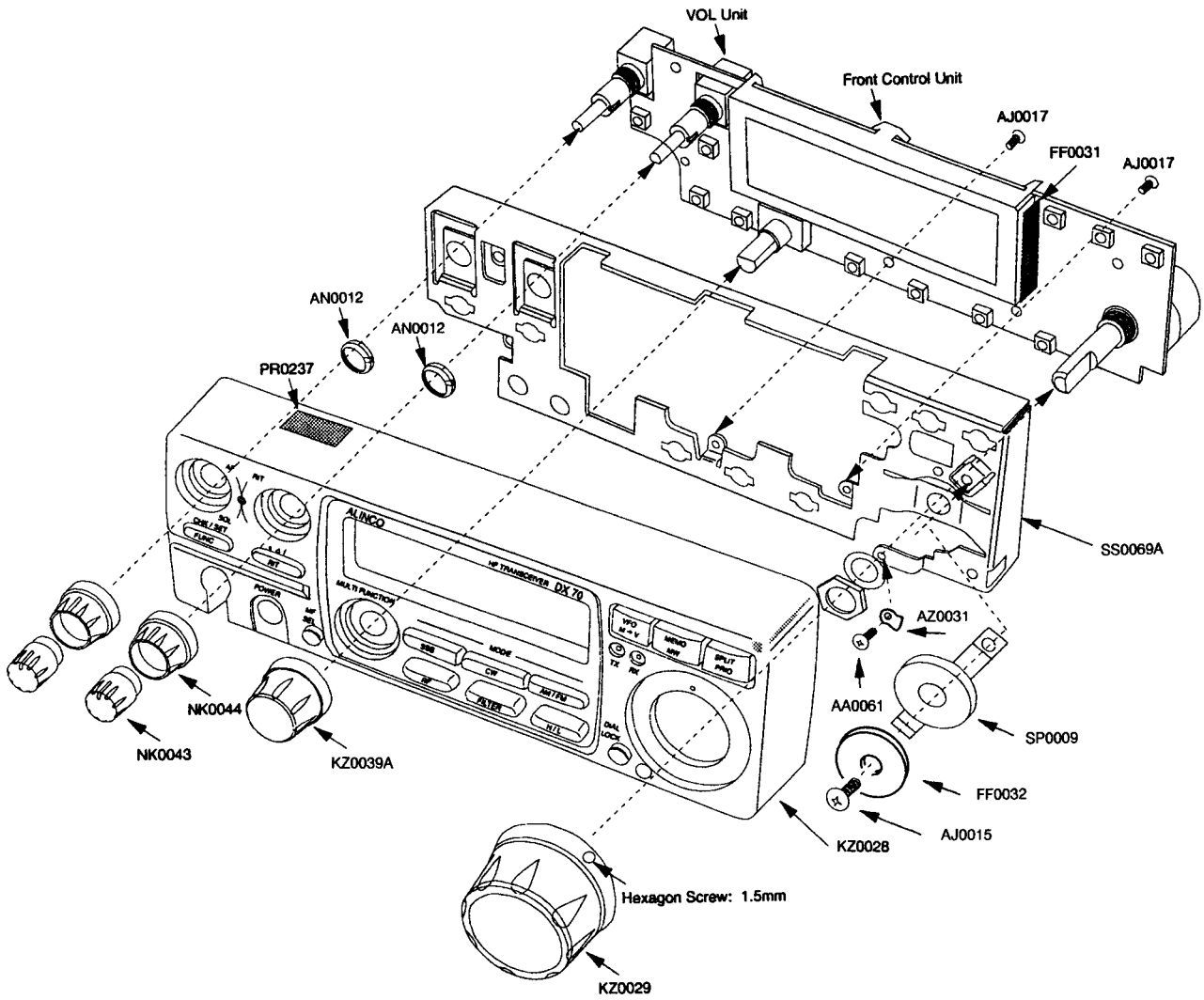
30) Transistor, Diode and LED Outline Drawings

Top View

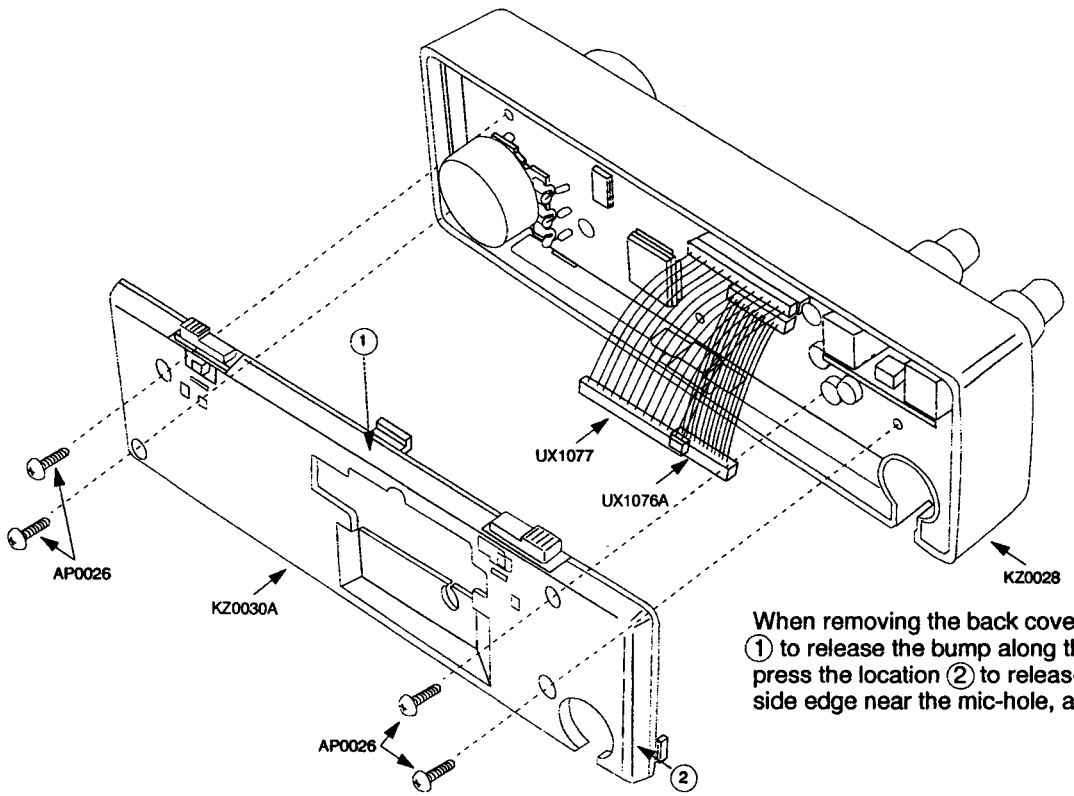


EXPLODED VIEW

1) Front Control Unit 1

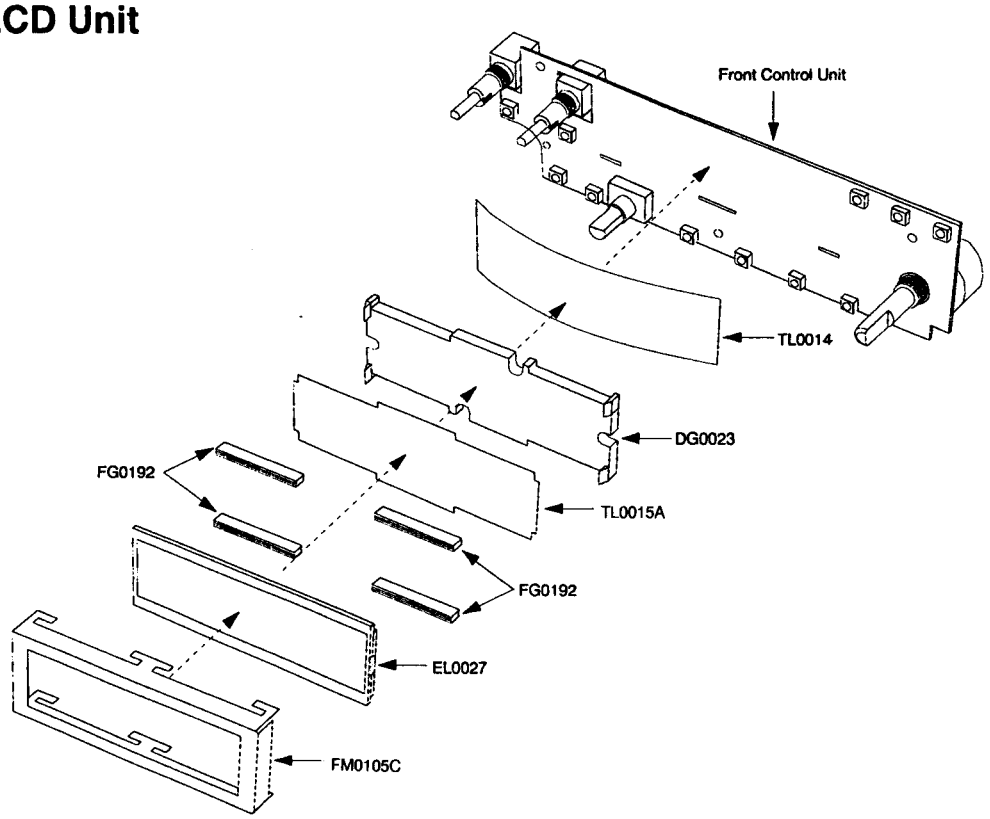


2) Front Control Unit 2

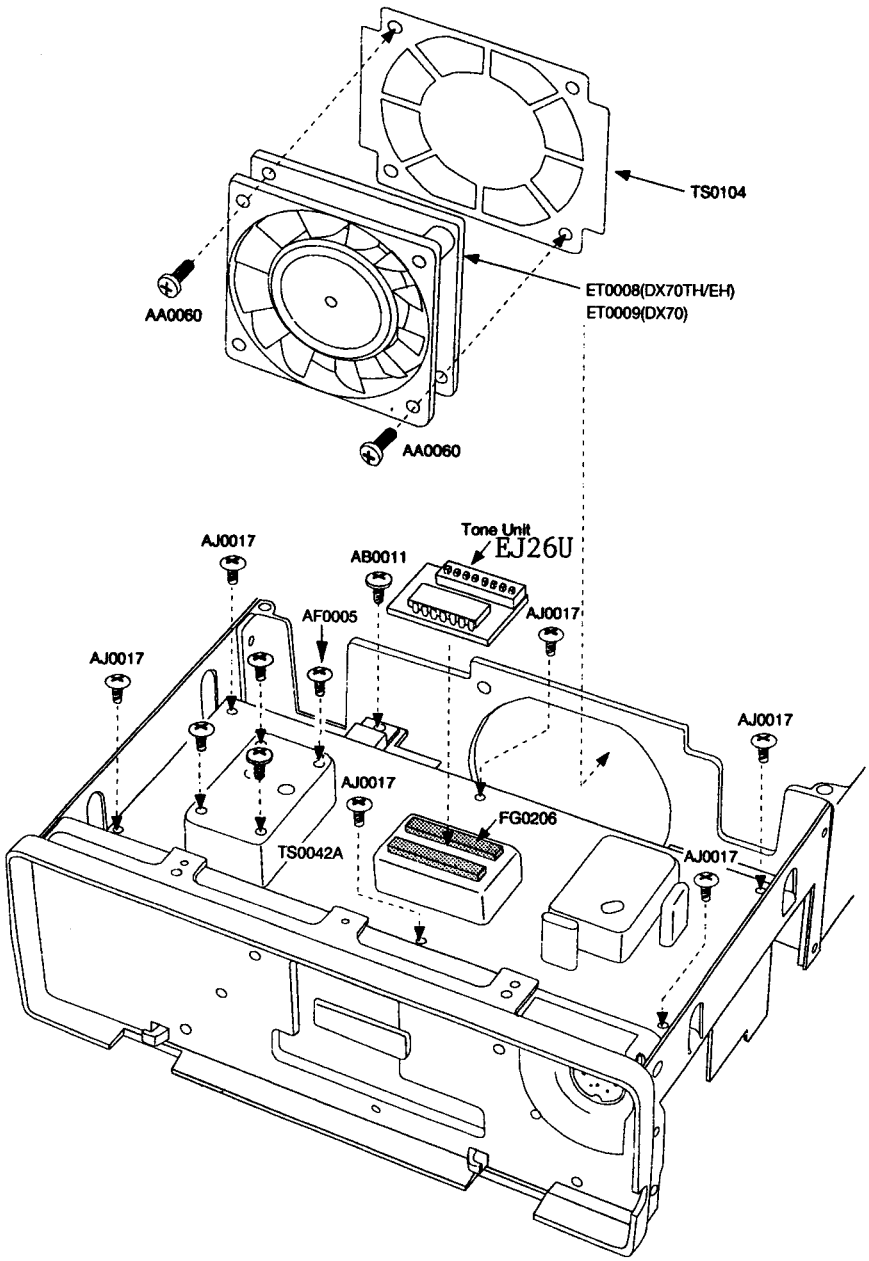


When removing the back cover, press the location ① to release the bump along the top edge, then press the location ② to release the bump along the side edge near the mic-hole, and open.

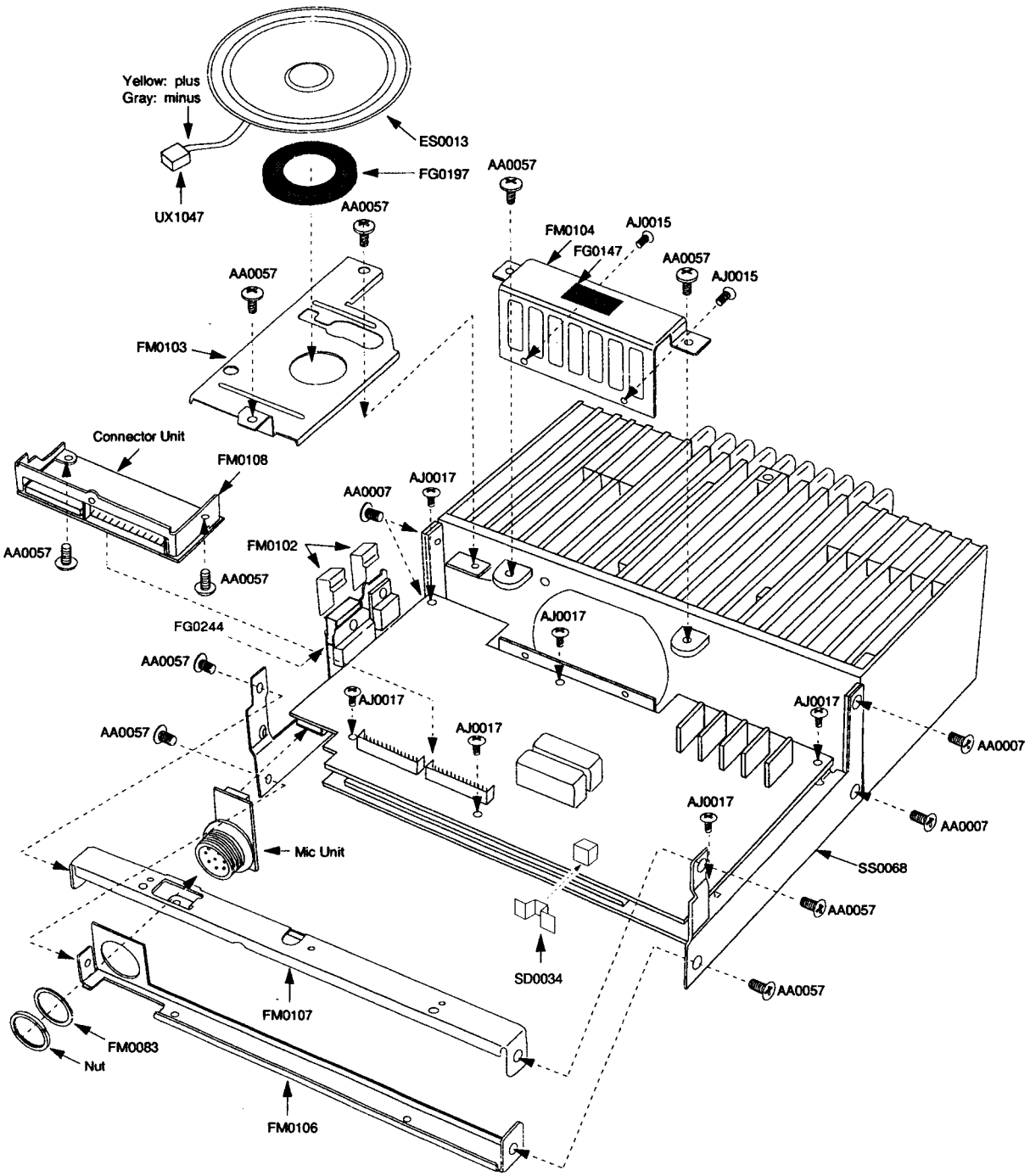
3) LCD Unit



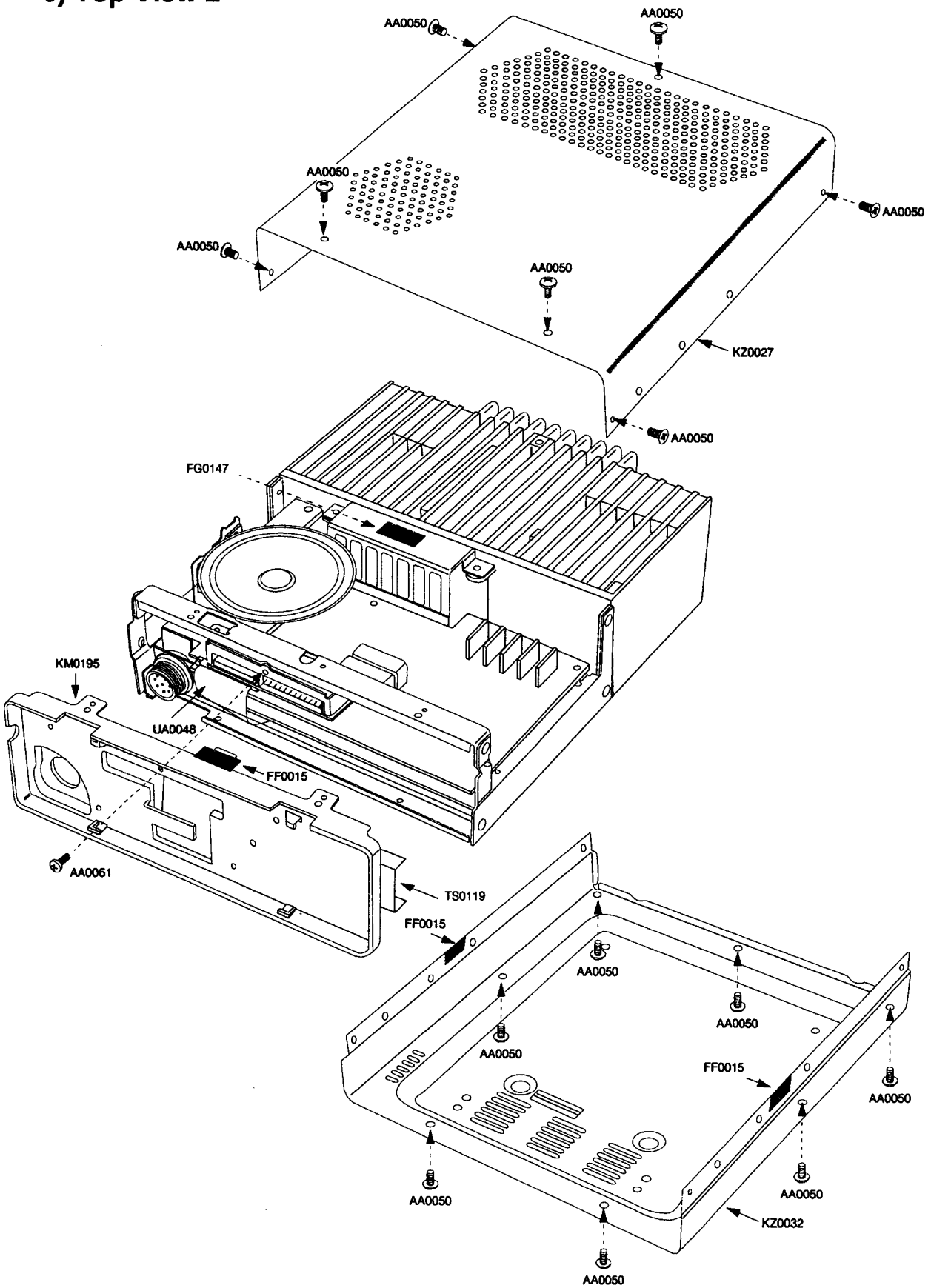
4) PLL Unit and Fan



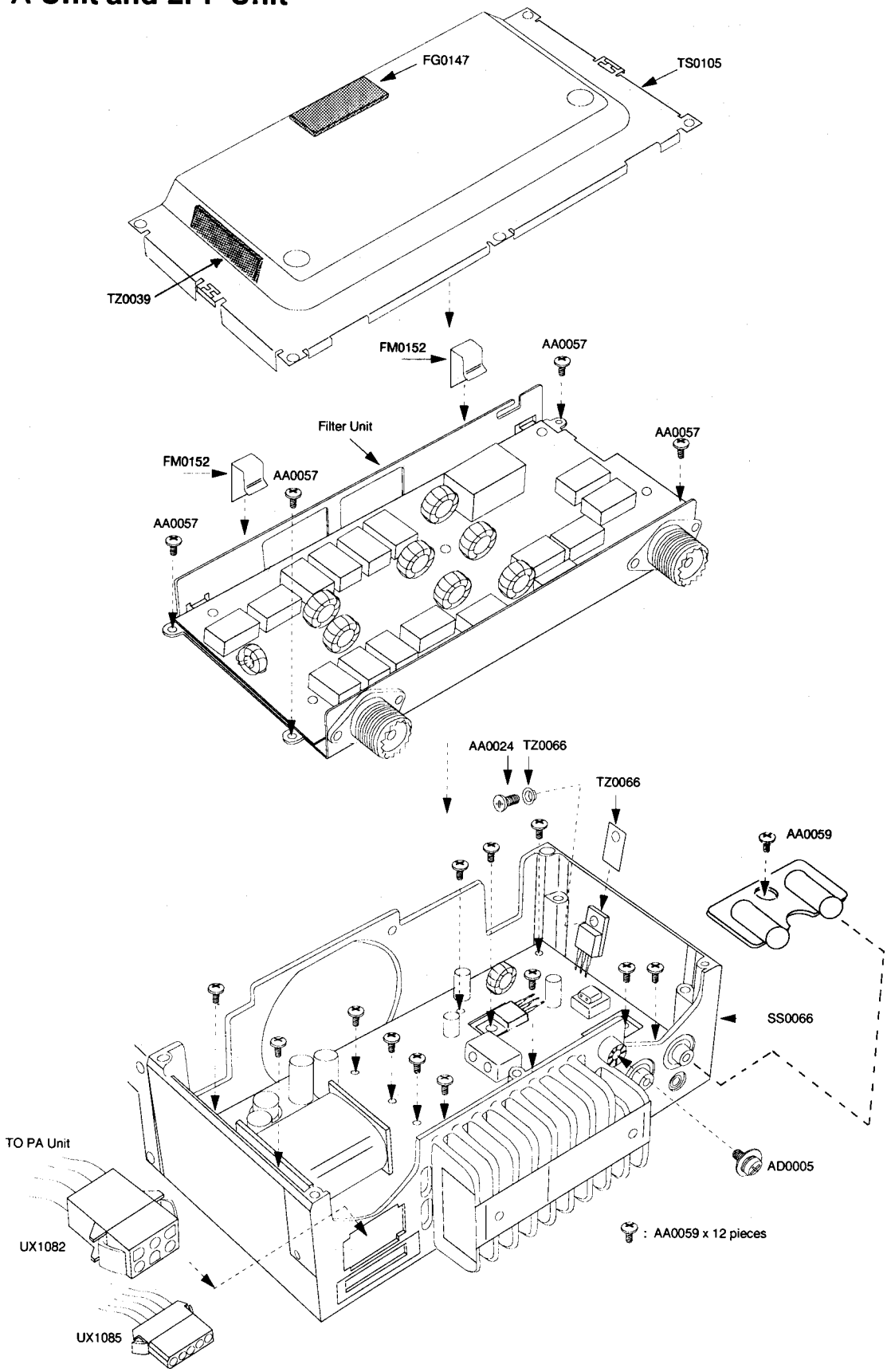
5) Top View 1


Yellow: plus
Gray: minus
UX1047
ES0013
FG0197
AA0057
AA0057
AA0057
FM0104
AJ0015
FG0147
AA0057
AJ0015
FM0103
Connector Unit
FM0108
AA0057
AA0057
AA0007
AJ0017
FM0102
FG0244
AA0057
AJ0017
AJ0017
AJ0017
AA0057
AJ0017
AJ0017
AA0007
AA0007
Mic Unit
SS0068
AA0057
SD0034
AA0057
FM0107
FM0083
Nut
FM0106

6) Top View 2


AA0050
AA0050
AA0050
AA0050
AA0050
AA0050
AA0050
KZ0027
AA0050
FG0147
KM0195
UA0048
FF0015
AA0061
TS0119
FF0015
AA0050
AA0050
AA0050
FF0015
AA0050
AA0050
AA0050
KZ0032
AA0050

8) PA Unit and LPF Unit



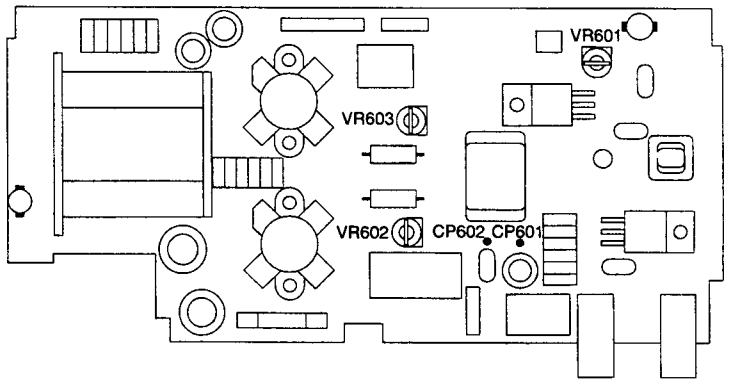
ADJUSTMENT

1) PA unit Adjustment

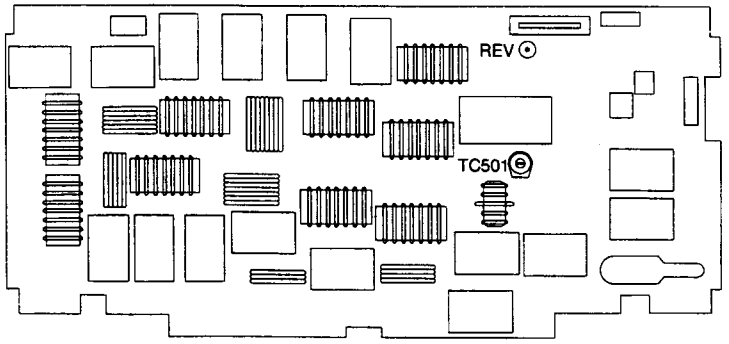
Required Test Equipment

1. Digital voltage meter
2. DC current meter — 300~500mA
   3A
3. DC regulated power supply — 13.80V 25A or more
   (should be equipped with 20~25A current limit and current meter)
4. Power meter — 100W (1.9~60MHz)
5. Linear detector
6. SG or RF generator — 1.9~60MHz, -10~+10dBm

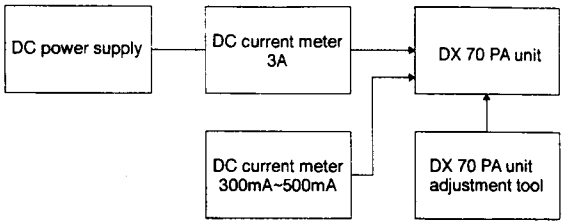
PA Unit Adjustment Points



Filter Unit Adjustment Points

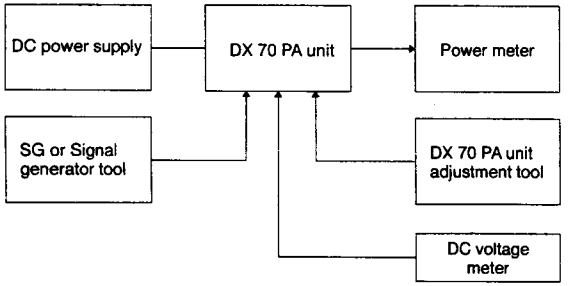


Idle Current Adjustment Setting



Adjustment the idle current without input signal.

SWR Adjustment Setting



Adjust SWR at approximately 50W.

PA Adjustment

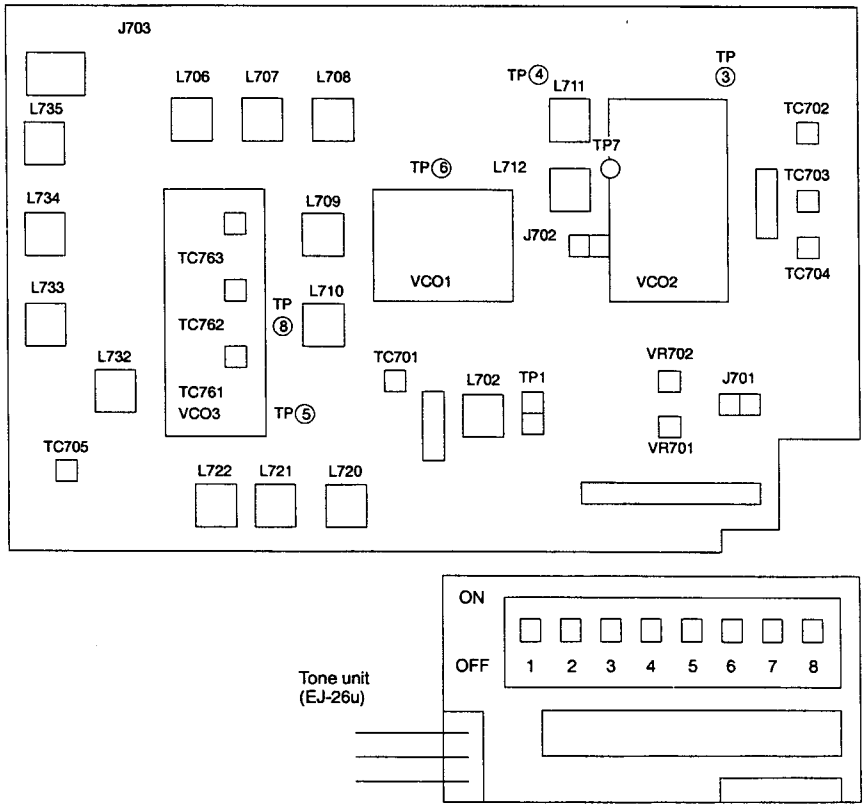
Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
Idling current 2SC1972 x 2	SSG: OFF Mode: USB VR601, 602, 603: min.	Current Meter 300~500mA	CP601 ⊖ CP602 ⊕	PA	VR601	Connect the current meter between CP601 and CP602, then adjust VR601 to 100mA.
Idling current MRF255 x 2	SSG: OFF Mode: USB	Current Meter 3A	CN605 unit total current		VR602 VR603	Turn VR602 and VR603 counterclockwise fully, check the total current in transmission mode. Turn VR602 clockwise slowly so that the total current increases 400mA. Then turn VR603 clockwise slowly so that the total current increases 400mA. As a result, the total current increases 800mA.
Connect TP1and TP2 by soldering after adjusting.						
SWR detection	f=1.9MHz SG >>PA unit	Voltage Meter	REV	Filter	TC501	Adjust the output power to 50W, then adjust the TC501 so that REV voltage is min.
	When you adjust the finished goods, set the mode to SSB, adjust the input level of microphone, and set the output power to about 50W.					

2) PLL Adjustment

Required Test Equipment

1. Digital voltage meter
2. DC regulated power supply 13.80V 5A or more
3. Frequency counter 500MHz or more
4. Spectrum Analyzer 1GHz or more
5. Oscilloscope 100MHz or more

PLL Unit Adjustment Points



Item	Condition	Measurement			Adjustment		
		Equipment	Unit	Terminal	Unit	Parts	Method
VCO1 Frequency	PD1=1.2V	Freq. Counter	VCO1	CN90 1~3			175MHz or above
	PD1=4.3V						155MHz or below
VCO2 Frequency	PD1=1.5~4V	Freq. Counter	VCO2	CN90 2~4			VCO2 freq.: 71MHz
Attach the VCO to PLL, then adjust the unit after installing the PLL to the unit.							
VCO2 Lock range	f=7.100MHz	Digital tester	PLL	TP7		Check	1.5V~4V
VCO1 Lock range	f=7.0999MHz			TP6			1V~3V
	f=7.1000MHz						3V~4.3V
VCO3 Lock range	f=0.1500MHz			TP8	VCO3	TC961	2.5V
	f=10.4999MHz					TC961	When the voltage is 6.45V or below, adjust the unit to 6.5V again. (6.45V~7.0V)
	f=10.5000MHz					TC962	2.5V
	f=21.4999MHz					TC962	When the voltage is 6.45V or below, adjust the unit to 6.5V again. (6.45V~7.0V)
	f=21.5000MHz					TC963	2.5V
	f=29.9999MHz					Check	6.5V or below
2nd LO Level	f=7.100MHz	Oscilloscope		TP4	PLL	L711 L712	Turn the coils to the max. repeatedly.
1st LO Level	f=7.100MHz			TP5		L709 L710	Turn the coils to the max. repeatedly.
	f=7.100MHz					L706 L707 L708	Turn the coils to the max. repeatedly.

Item	Condition	Measurement			Adjustment		
		Equipment	Unit	Terminal	Unit	Parts	Method
Frequency (Mode)	RX LSB	Freq. Counter	PLL	TP3	PLL	TC702	9873.60kHz +/- 0.02kHz
	RX USB					TC704	9876.40kHz +/- 0.02kHz
	RX AM and FM					TC703	9875.00kHz +/- 0.02kHz
	RX CWU					Check	9875.80kHz +/- 0.3kHz
	RX CWL						9874.20kHz +/- 0.3kHz
Frequency (IF Shift)	RX LSB			J701		VR702	453.60kHz +/- 0.1kHz
	TX LSB					VR701	453.60kHz +/- 0.01kHz
	RX LT, (IF Shift center)					Check	453.30kHz +/- 0.2kHz
	TX LT, (IF Shift center)						453.50kHz +/- 0.2kHz
	RX UT, (IF Shift center)						456.70kHz +/- 0.2kHz
	TX UT, (IF Shift center)						456.50kHz +/- 0.2kHz
Frequency	f=7.1000MHz, FM			J703		TC701 L702	78850.00kHz Adjust TC701 at first, then L702 when TC701 can not be adjusted.
Level	f=7.100MHz, USB	Spectrum Analyzer		J701		Check	-6~0dBm f=456.4kHz
Level	f=7.100MHz, USB			J702			1~6dBm f=71.295MHz
Level	f=53.9999MHz			J703		L720 L721 L722	Turn the coils to the max. repeatedly. f=123.75MHz
Level	f=53.9999MHz					L732 L733 L734 L745	Turn the coils to the max. repeatedly f=123.75MHz 1~6dBm
Spurious	f=53.9999MHz					TC705	Spurious min. (60dB or more)
Level	f=150kHz f=10.400MHz f=10.500MHz f=21.400MHz f=21.500MHz f=29.9999MHz					Check	Level: 2~6dBm +/-2dB

3) Tone Unit Adjustment

1 Attach EJ26U to DX70.
2 When the subaudible Tone is ON in FM mode, adjust the unit according to following table.
3 When the subaudible Tone is OFF in FM mode, the tone should not be emitted.

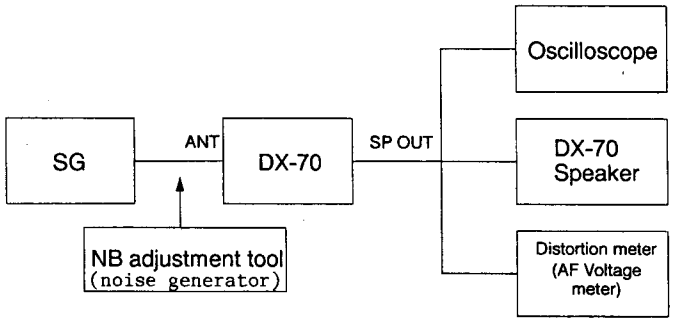
Item	Condition	Measurement			Adjustment		
		Equipment	Unit	Terminal	Unit	Parts	Method
Tone Frequency	250.3Hz 1 2 3 4 5 6 7 8 * * *	Freq. Counter	EJ26 u	CN99 1~1			249.6~251.0Hz
Tone Frequency	156.3Hz 1 2 3 4 5 6 7 8 * * *	Freq. Counter	EJ26 u	CN99 1~1			156.2~157.2Hz
Tone Level	156.3Hz 1 2 3 4 5 6 7 8 * * *	Oscilloscope	EJ26 u	CN99 1~1			1.8~3.0V p-p
Tone Level	156.3Hz 1 2 3 4 5 6 7 8 * * * *	Oscilloscope	EJ26 u	CN99 1~1			2.8~3.8V p-p
Tone Level	156.3Hz 1 2 3 4 5 6 7 8 * * * * *	Oscilloscope	EJ26 u	CN99 1~1			3.8~4.8V p-p
Final Setting	88.5Hz 1 2 3 4 5 6 7 8 * *						Attach to the DX70T after the tone level obtains 88.5Hz.

* indicates the number is ON.

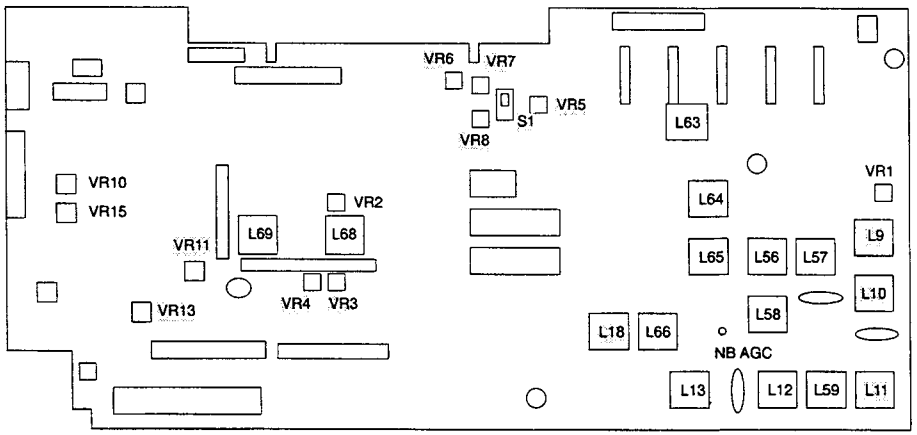
Required Test Equipment

1. Digital voltage meter
2. DC regulated power supply — 13.80V 3A or more
3. SG — about 200MHz
4. Distortion meter, AF voltage meter
5. 8Ω speaker
6. Oscilloscope
7. (NB adjustment tool)

Main Unit Adjustment Setting



Main Unit Adjustment Points



TX Adjustment

4) Sensitivity Adjustment

SG Output Frequency: 14.1000MHz
Frequency: 14.0993MHz — Mode: USB
RF Gain: +10dB — ΔIF: Center
Filter: Wide

Connect to HF Antenna Terminal.
RIT: OFF — AGC: FAST — NB: OFF
Squelch VR: Turn the knob counterclockwise fully.

Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
Tuning	SG output: 0dBμ Mod: OFF AF output: 300mV	Audio Voltmeter	SP	Main	L56 L57 L58 L59 L12 L13 L66 L68 L69	Adjust every following group repeatedly to obtain the maximum receiving signal; L56, 57, 58 L59, 12, 13 L66 L68, L69
	Mode: FM f=14.1000MHz SG output: 0dBμ Mod: 1kHz, 3.5kHzDEV	Distortion Meter			L59 L12 L13	Adjust repeatedly to obtain the maximum SINAD. SINAD should be 13dB or more.
	SG output: 60dBμ 1kHz, 3.5kHzDEV				Check	SINAD should be 30dB or more. If SINAD is below 30dB, adjust L59, L12 and L13 again.
	SG output: -6dBμ Mod: OFF Mode: USB f=14.0993MHz AF output: 300mV	Audio Voltmeter			Check	Make sure that S/N is 10.5dB or more by turning ON/OFF SG output.
	SG output: 10dBμ Mod: 1kHz, 30% Mode: AM f=14.1000MHz				Check	Make sure S/N is 10dB or more by turning ON/OFF SG modulation.

5) Noise Blanker Adjustment

SG Output Frequency: 14.1000MHz
Frequency: 14.0993MHz Mode: USB
RF Gain: +10dB ΔIF: Center
Filter: Wide

Connect to HF Antenna Terminal.
RIT: OFF AGC: FAST NB: OFF
Squelch VR: Turn the knob counterclockwise fully.

Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
Tuning	SG output: 0dBμ Mod: OFF Mode: USB f=14.0993MHz NB: ON RF Gain: +10dB	Oscilloscope	NB AGC (MAIN)	Main	L63 L64 L65	Adjust the coils, and set DC voltage of the terminal to the minimum with the oscilloscope.

6) S Meter Adjustment

Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
RX Total Gain	SG output: 40dBμ Mod: OFF Mode: USB f=14.0993MHz RF Gain: 0dB	AF Voltmeter	SP	Main	VR2	Adjust SP output by setting the AF gain to about 1V. The output level should be 0dB. Adjust only the noise output to -28dB by turning OFF SG output.
S Meter	SG output: 20dBμ Mod: OFF SG output: 40dBμ	S Meter	S Meter		VR10 VR15	The indicator between first and second digits is turned ON. The 9th digit starts flashing. Adjust VR10 and VR15 repeatedly.
	SG: OFF				Check	S Meter is not turned ON.
Squelch	SG: OFF		BUSY RX LED (Green) AF output		Check	Turn the Squelch VR to make sure that the squelch closes at about 10 o'clock.

7) Receiving Function Adjustment

SG Output Frequency: 14.1000MHz
Frequency: 14.0993MHz Mode: USB
RF Gain: +10dB ΔIF: Center
Filter: Wide

Connect to HF Antenna Terminal.
RIT: OFF AGC: FAST NB: OFF
Squelch VR: Turn the knob counterclockwise fully.

Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
AGC	SG output: 40dBμ Output: ON/OFF Mod: OFF		S Meter		Check	Switch AGC. When SG is turned OFF, the meter moves slowly in SLOW, and fast in FAST.
RF GAIN	SG output: 40dBμ		S Meter		Check	Switch the RF GAIN from +10dB orderly, the meter swings shorter and shorter.
FILTER Switching	Output: OFF Mode: USB, AM, CW				Check	Switch the FILTER in every mode (except FM), the noise sound should be changed.
Band Sensitivity	SG output: -6dBμ f=1.9000MHz f=3.6000MHz f=7.0000MHz f=10.1000MHz f=21.1000MHz f=28.1000MHz Mode: USB or LSB	Audio Voltmeter	SP		Check	In USB mode, SG frequency is -700Hz. In LSB mode, SG frequency is +700Hz. Make sure that S/N is 10dB or more.
50MHz Sensitivity	Connect SG to 50MHz antenna terminal. SG output: -10dBμ SG freq.: 52.1000MHz Mode: USB f=52.0993MHz				Check	S/N is 10.5dB or more when turning ON/OFF SG output.
	SG output: -4dBμ Mod: 1kHz, 3.5kHzDev Mode: FM f=52.0000MHz	Distortion Meter			Check	SINAD: 13dB or more

5) Noise Blanker Adjustment

SG Output Frequency: 14.1000MHz
Frequency: 14.0993MHz Mode: USB
RF Gain: +10dB ΔIF: Center
Filter: Wide

Connect to HF Antenna Terminal.
RIT: OFF AGC: FAST NB: OFF
Squelch VR: Turn the knob counterclockwise fully.

Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
Tuning	SG output: 0dBμ Mod: OFF Mode: USB f=14.0993MHz NB: ON RF Gain: +10dB	Oscilloscope	NB AGC (MAIN)	Main	L63 L64 L65	Adjust the coils, and set DC voltage of the terminal to the minimum with the oscilloscope.

6) S Meter Adjustment

Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
RX Total Gain	SG output: 40dBμ Mod: OFF Mode: USB f=14.0993MHz RF Gain: 0dB	AF Voltmeter	SP	Main	VR2	Adjust SP output by setting the AF gain to about 1V. The output level should be 0dB. Adjust only the noise output to -28dB by turning OFF SG output.
S Meter	SG output: 20dBμ Mod: OFF SG output: 40dBμ	S Meter	S Meter		VR10 VR15	The indicator between first and second digits is turned ON. The 9th digit starts flashing. Adjust VR10 and VR15 repeatedly.
	SG: OFF				Check	S Meter is not turned ON.
Squelch	SG: OFF		BUSY RX LED (Green) AF output		Check	Turn the Squelch VR to make sure that the squelch closes at about 10 o'clock.

7) Receiving Function Adjustment

SG Output Frequency: 14.1000MHz
Frequency: 14.0993MHz Mode: USB
RF Gain: +10dB ΔIF: Center
Filter: Wide

Connect to HF Antenna Terminal.
RIT: OFF AGC: FAST NB: OFF
Squelch VR: Turn the knob counterclockwise fully.

Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
AGC	SG output: 40dBμ Output: ON/OFF Mod: OFF		S Meter		Check	Switch AGC. When SG is turned OFF, the meter moves slowly in SLOW, and fast in FAST.
RF GAIN	SG output: 40dBμ		S Meter		Check	Switch the RF GAIN from +10dB orderly, the meter swings shorter and shorter.
FILTER Switching	Output: OFF Mode: USB, AM, CW				Check	Switch the FILTER in every mode (except FM), the noise sound should be changed.
Band Sensitivity	SG output: -6dBμ f=1.9000MHz f=3.6000MHz f=7.0000MHz f=10.1000MHz f=21.1000MHz f=28.1000MHz Mode: USB or LSB	Audio Voltmeter	SP		Check	In USB mode, SG frequency is -700Hz. In LSB mode, SG frequency is +700Hz. Make sure that S/N is 10dB or more.
50MHz Sensitivity	Connect SG to 50MHz antenna terminal. SG output: -10dBμ SG freq.: 52.1000MHz Mode: USB f=52.0993MHz				Check	S/N is 10.5dB or more when turning ON/OFF SG output.
	SG output: -4dBμ Mod: 1kHz, 3.5kHzDev Mode: FM f=52.0000MHz	Distortion Meter			Check	SINAD: 13dB or more

Connect the power meter to 50MHz antenna terminal.
Frequency: 52.000MHz Mode: USB Power: High
Speech Compressor (SET mode): OFF FM-TONE: OFF

Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
Filter Tuning	AG output: -30dBm Mode: FM FM-TONE: OFF	Oscilloscope (Linear Detector)	50MHz Antenna Terminal	Main	L11 L10 L9	Set the AM modulation factor to the minimum. It should be 5% or below.
Carrier Balance	AG output: OFF f: 7.1000MHz Mode: LSB/USB	Oscilloscope	HF Antenna Terminal		VR3 VR4	Adjust VR3 and VR4 so that the carrier suppression is 50dB (1/300) or below at 100W. The carrier suppression should be decreased in both USB and LSB.
CW Wave Form	Mode: CW-L/CW-U Electronic-keyer (dot): approx. 20mS				VR11 Check	Make sure of the wave form. The wave form of rise and fall should be symmetry. (The inclination is approx. 3mS.) The side tone of CW is should be heard from speaker.
Low Power	Mode: FM Power: Low	Power Meter			Check	Within 10~20W
AM Power	AG output: OFF Mode: AM Power: High				Check	35~50W
Band Power	Mode: FM Band (MHz): 1.9, 3.5, 10, 14,18,21,24,28,50				Check	Make sure that the power is 90~110W.

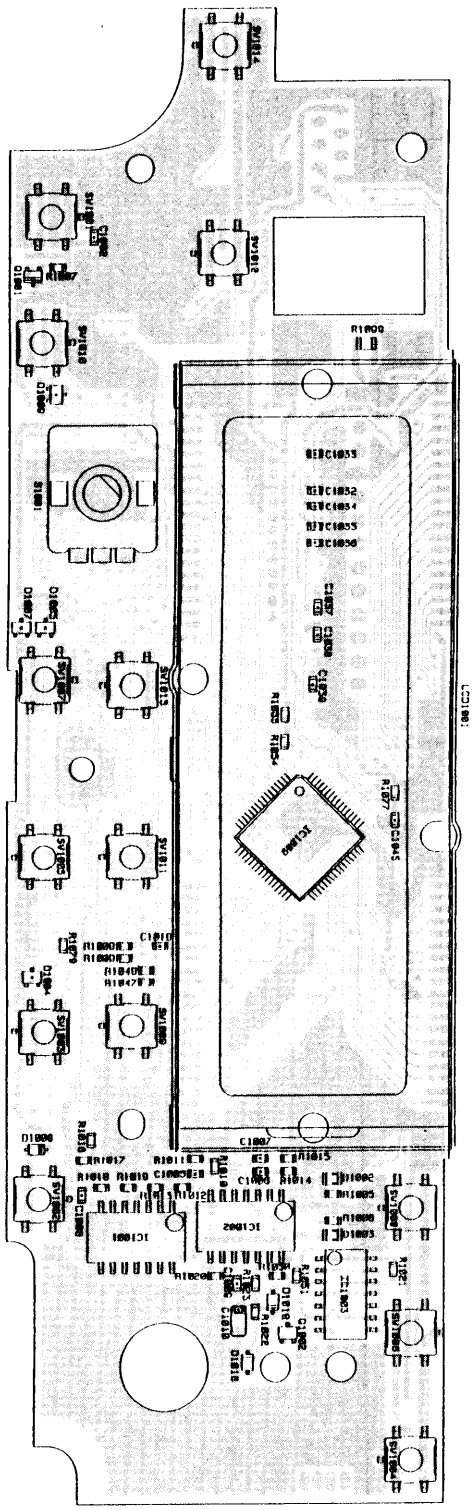
9) Spurious Adjustment

Connect the power meter to HF or 50MHz antenna terminal.
Frequency: 52.000MHz Mode: FM Power: High
Speech Compressor (SET mode): OFF FM-TONE: OFF

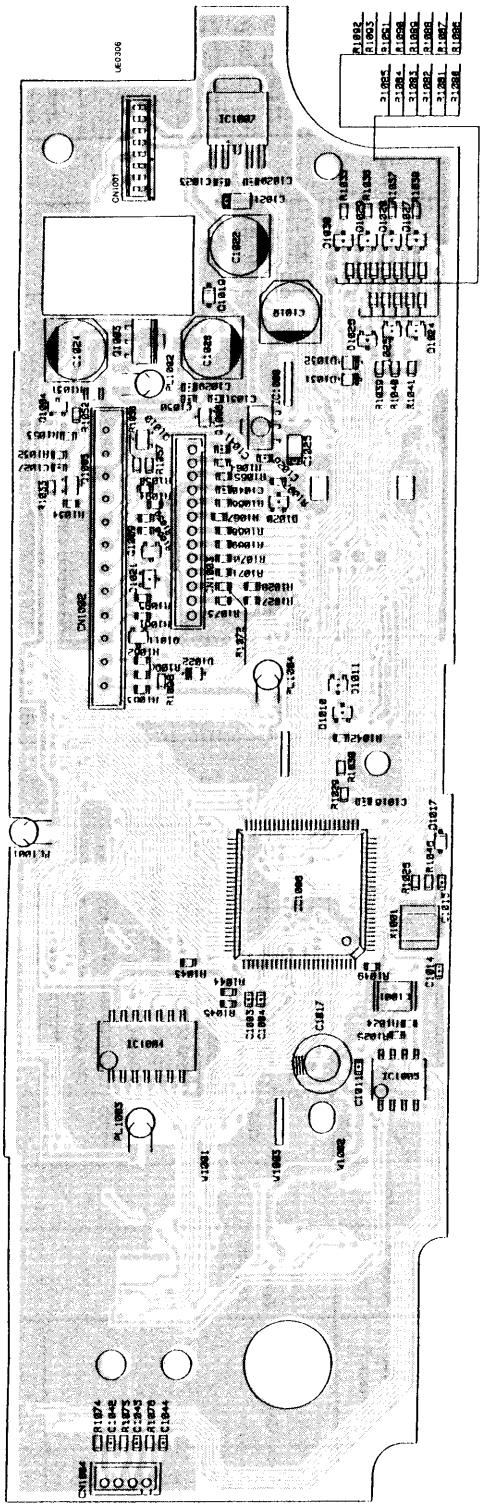
Item	Condition	Measurement		Adjustment		
		Equipment	Terminal	Unit	Parts	Method
Spurious Balance	AG output: OFF Mode: FM FM-TONE: OFF (f: 52.0000MHz)	ATT + spectrum Analyzer	50MHz Antenna Terminal	Main	VR1	Balance the spurious to obtain the minimum value. -60dB or below
Spurious	AG output: OFF Mode: FM Band (MHz): 1.9, 3.5, 10, 14, 18, 21, 24, 28		HF Antenna Terminal		Check	-52dB or below (-47dB or below in 10MHz band only)
					L9	Adjust so that the value is within the regulation. (Adjust L9 when the spurious is not -52dB or below in 24/28MHz band.)
Carrier Balance	AG output: OFF Mode: LSB/USB				Check (VR3 VR4)	-50dB or below (Adjust VR3 and VR4 when the carrier suppression is not -50dB or below.)
Modulation	Mode: CW Keying: OFF f: 53.99MHz				Check	-60dB or below
	Mode: FM, AM, USB/LSB Connect the microphone.	Monitor Transceiver			Check	Make sure the modulation sound in every mode.

PC BORD VIEW

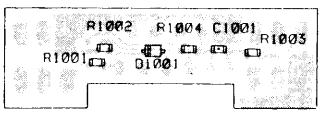
CPU Unit Side A (Later)



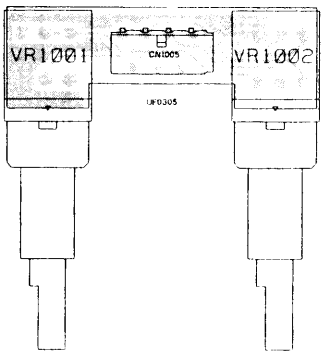
CPU Unit Side B (Later)



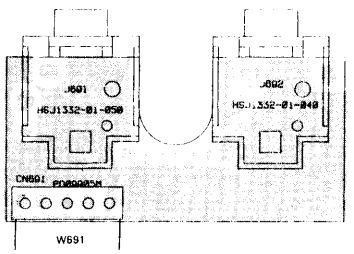
Vol. Unit Side A (Later)



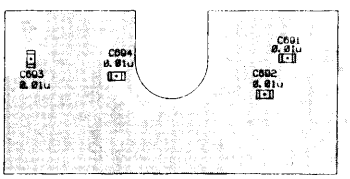
Vol. Unit Side B (Later)



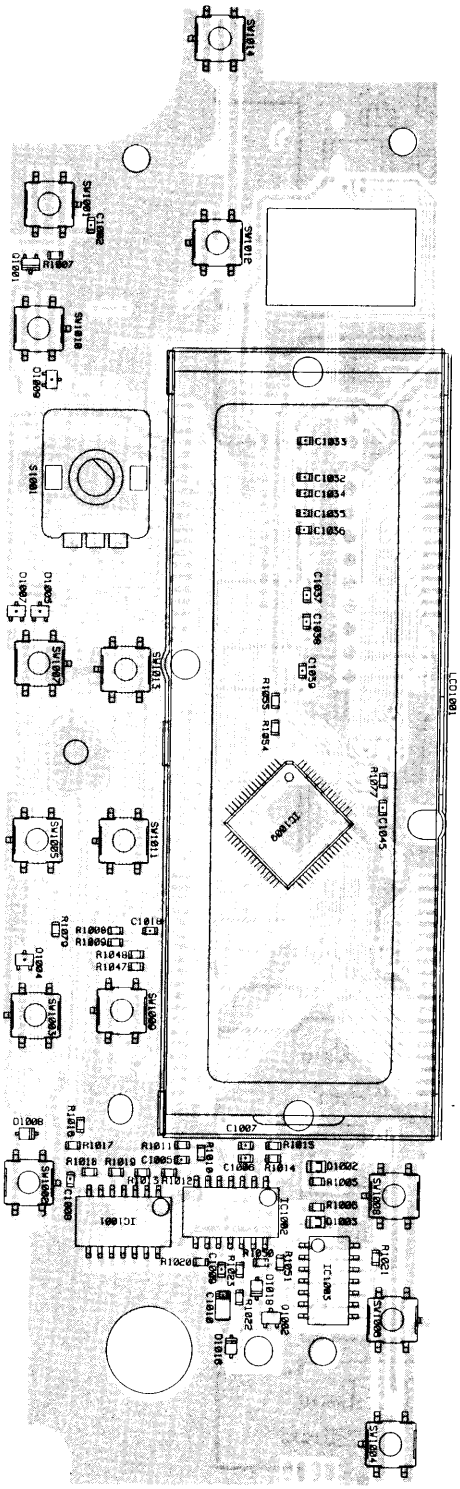
Jack Unit Side A



Jack Unit Side B



CPU Unit Side A (Early)



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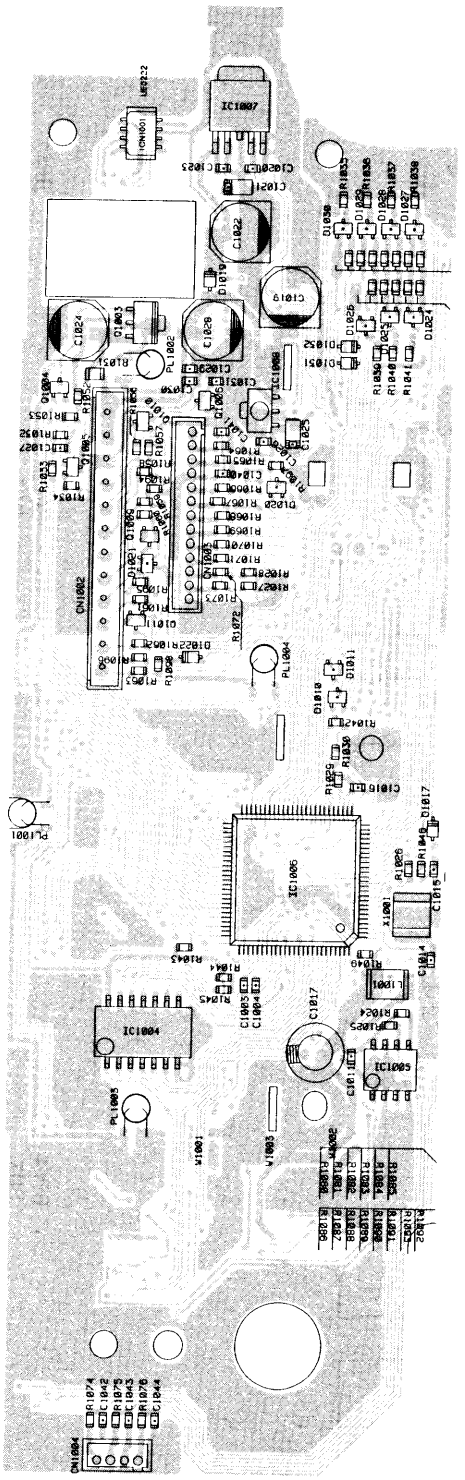
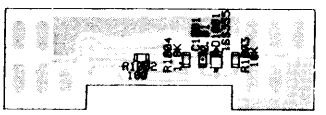
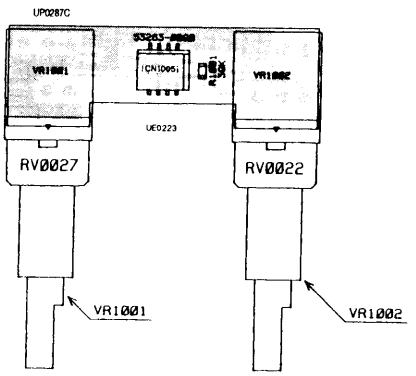


Vol. Unit Side A (Early)

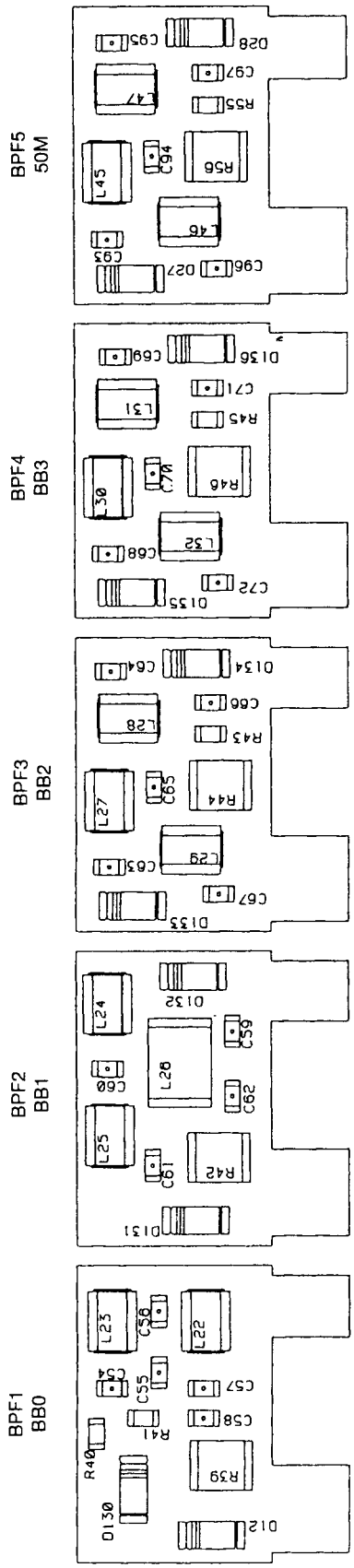
3) Vol. Unit Side A



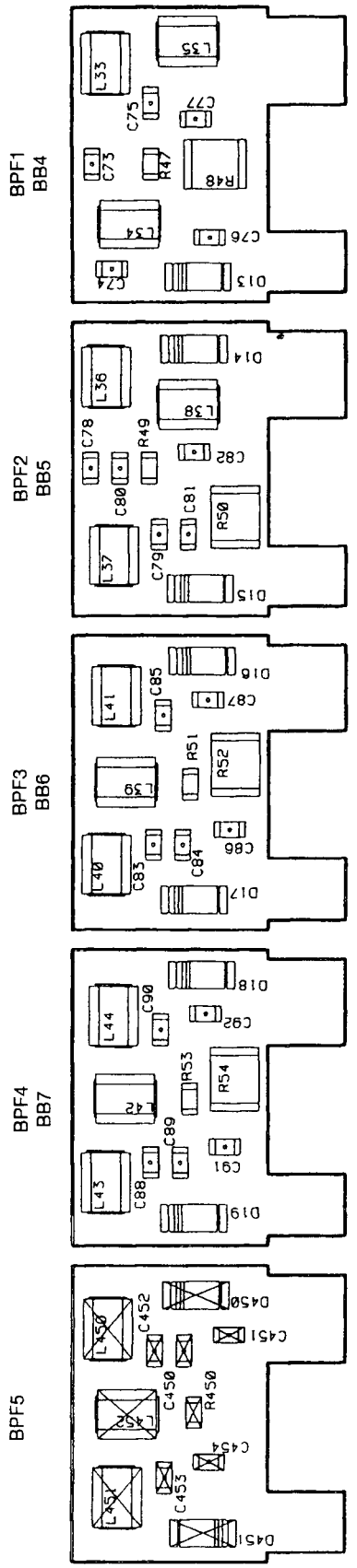
Vol. Unit Side B (Early)



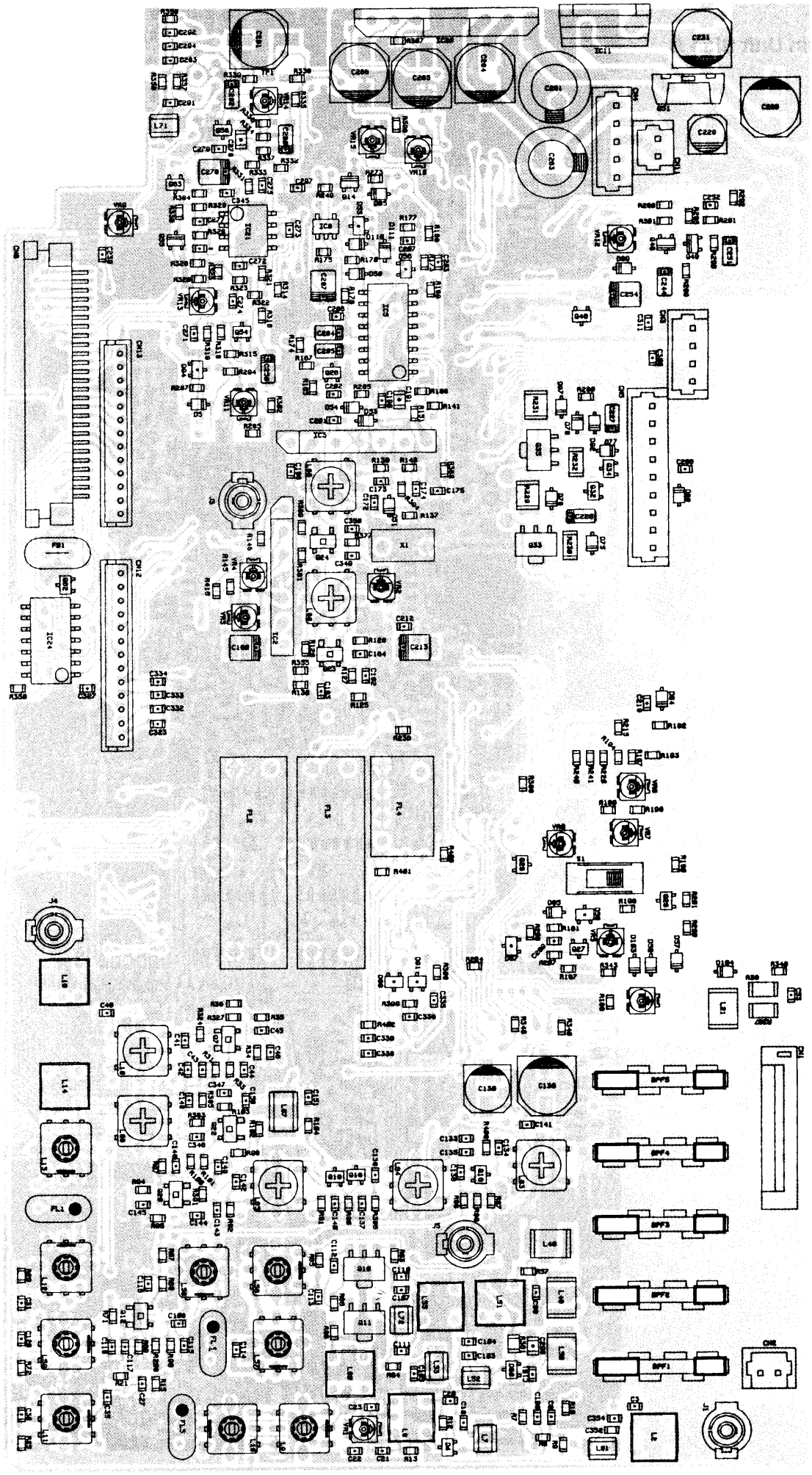
BPF UNIT Side A



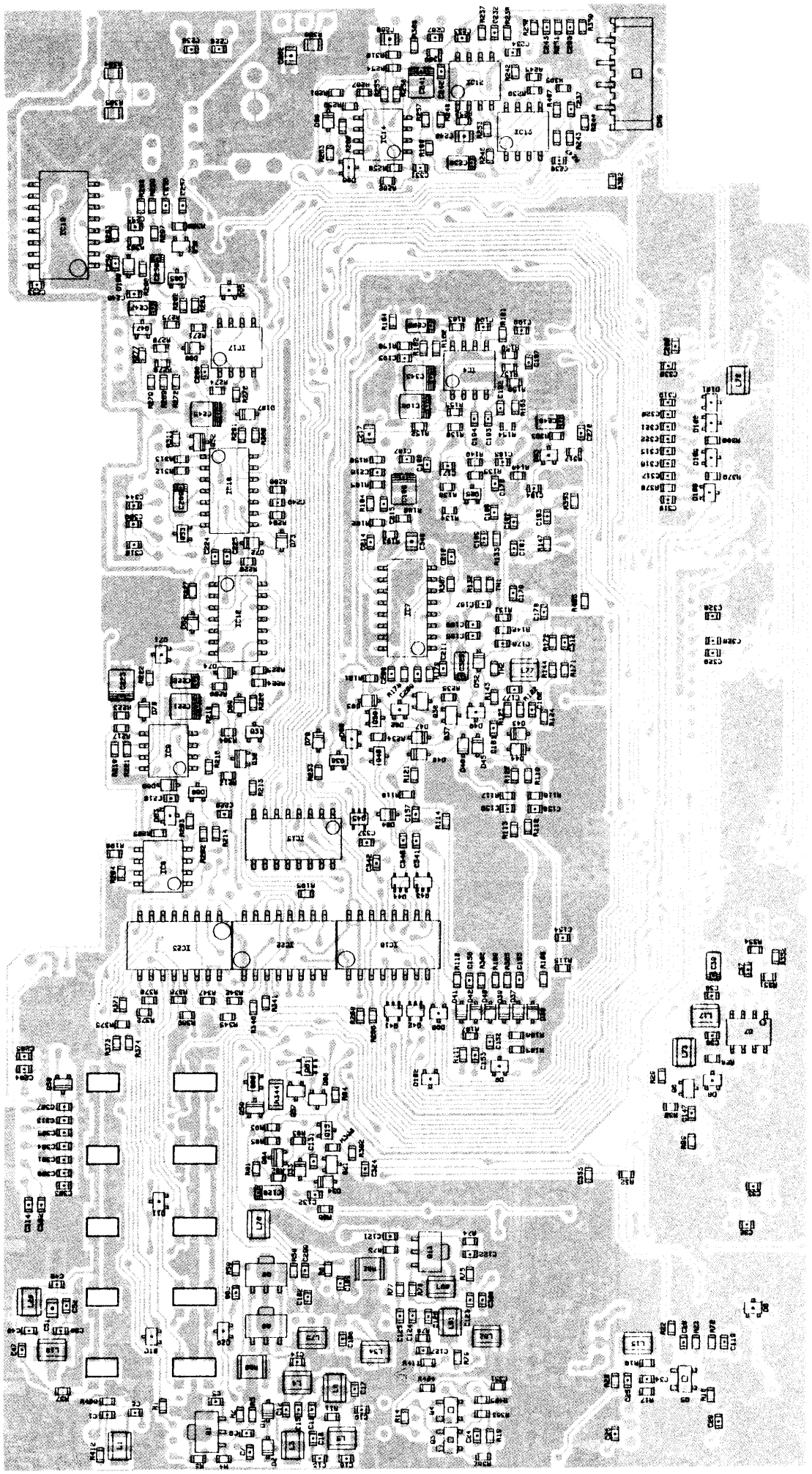
BPF UNIT Side B



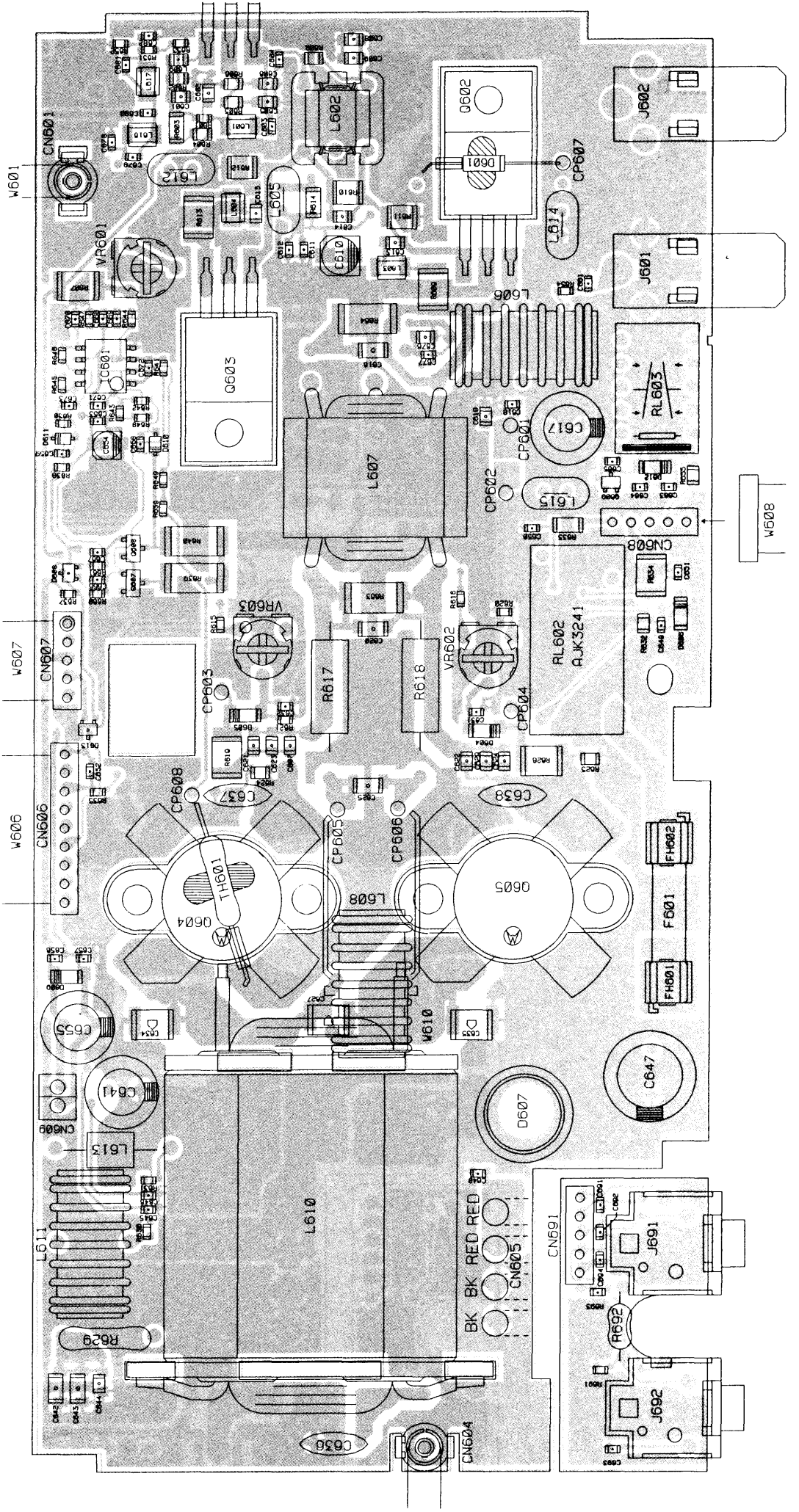
Main Unit Side A



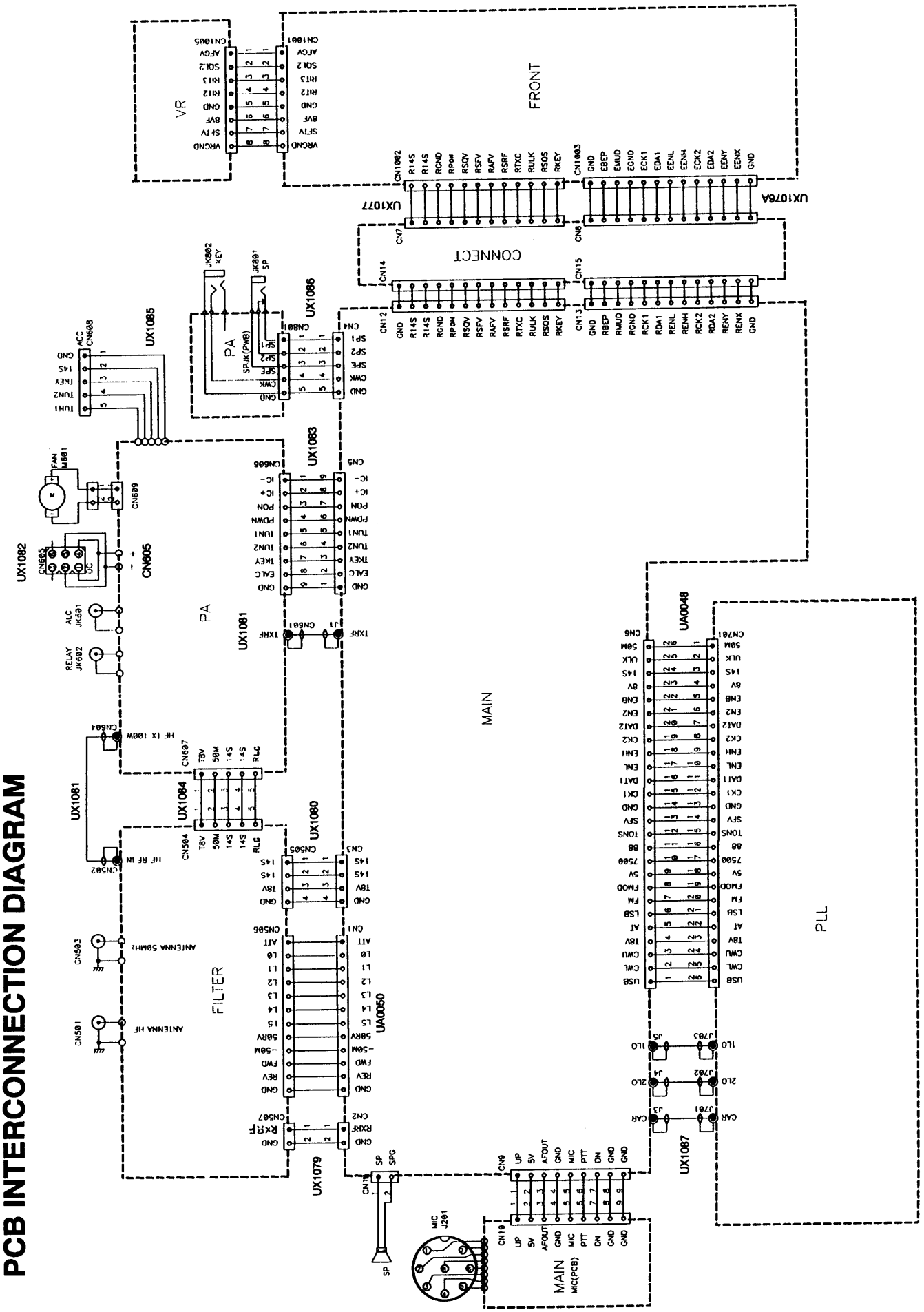
Main Unit Side B



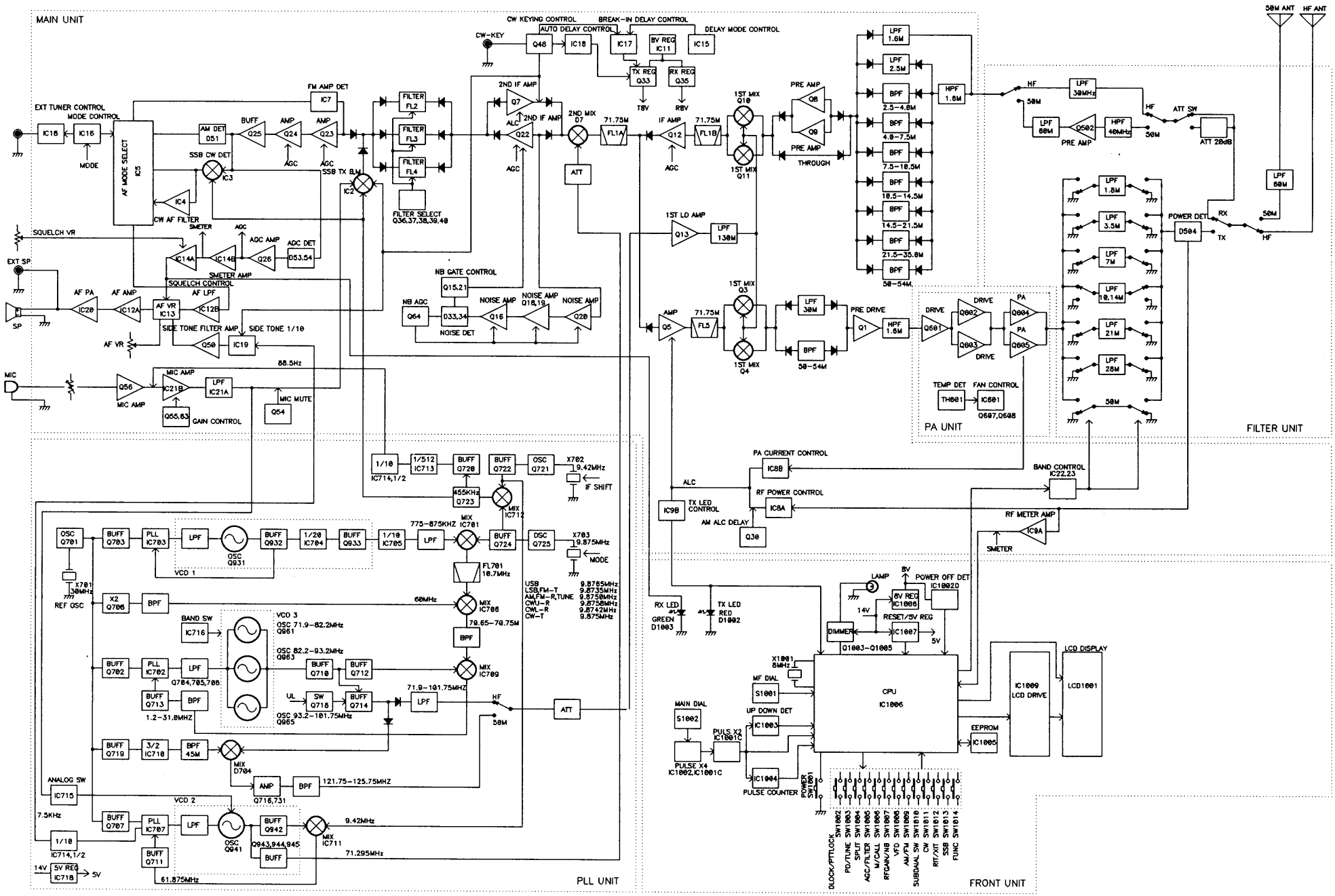
PA Unit Side A



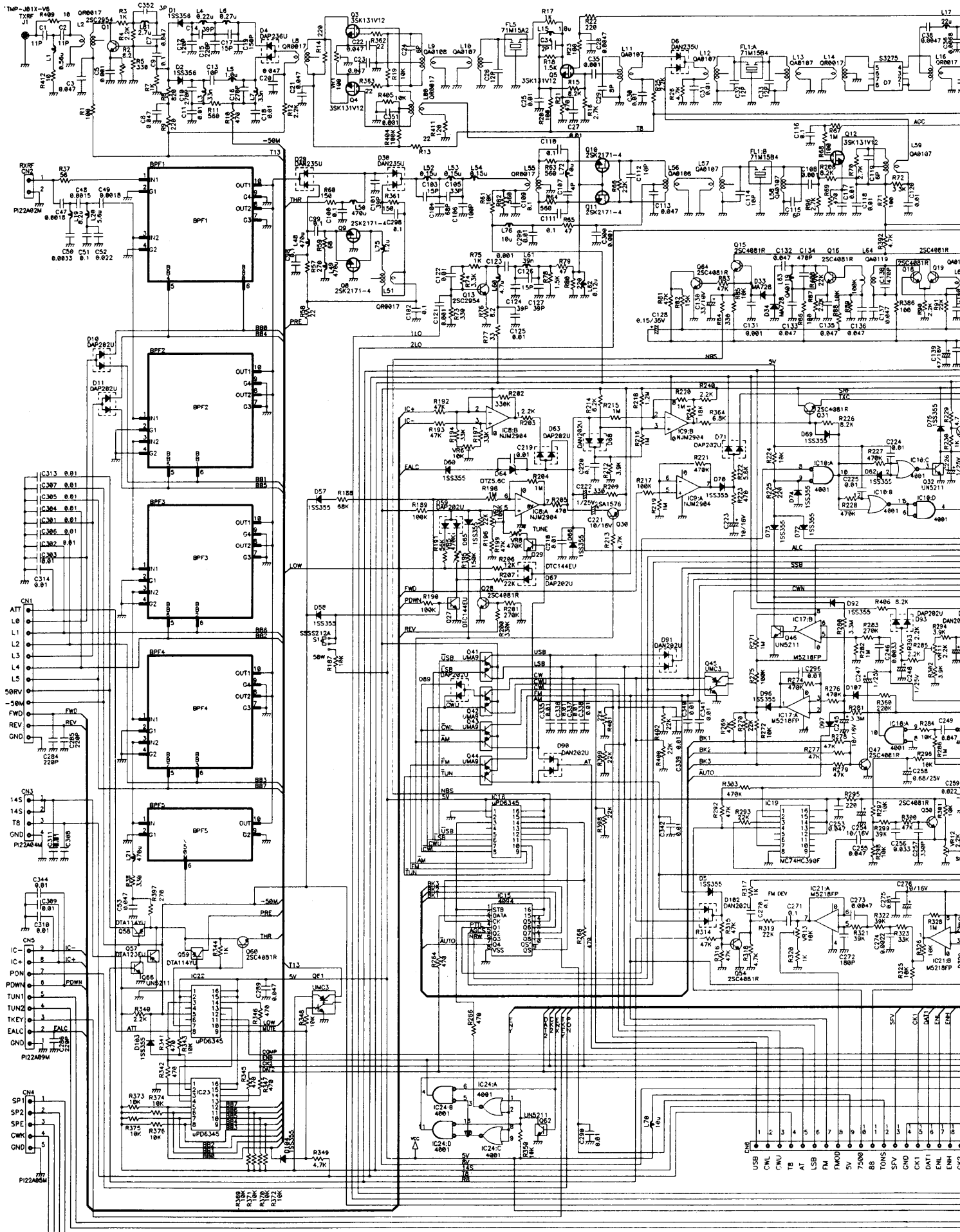
PCB INTERCONNECTION DIAGRAM

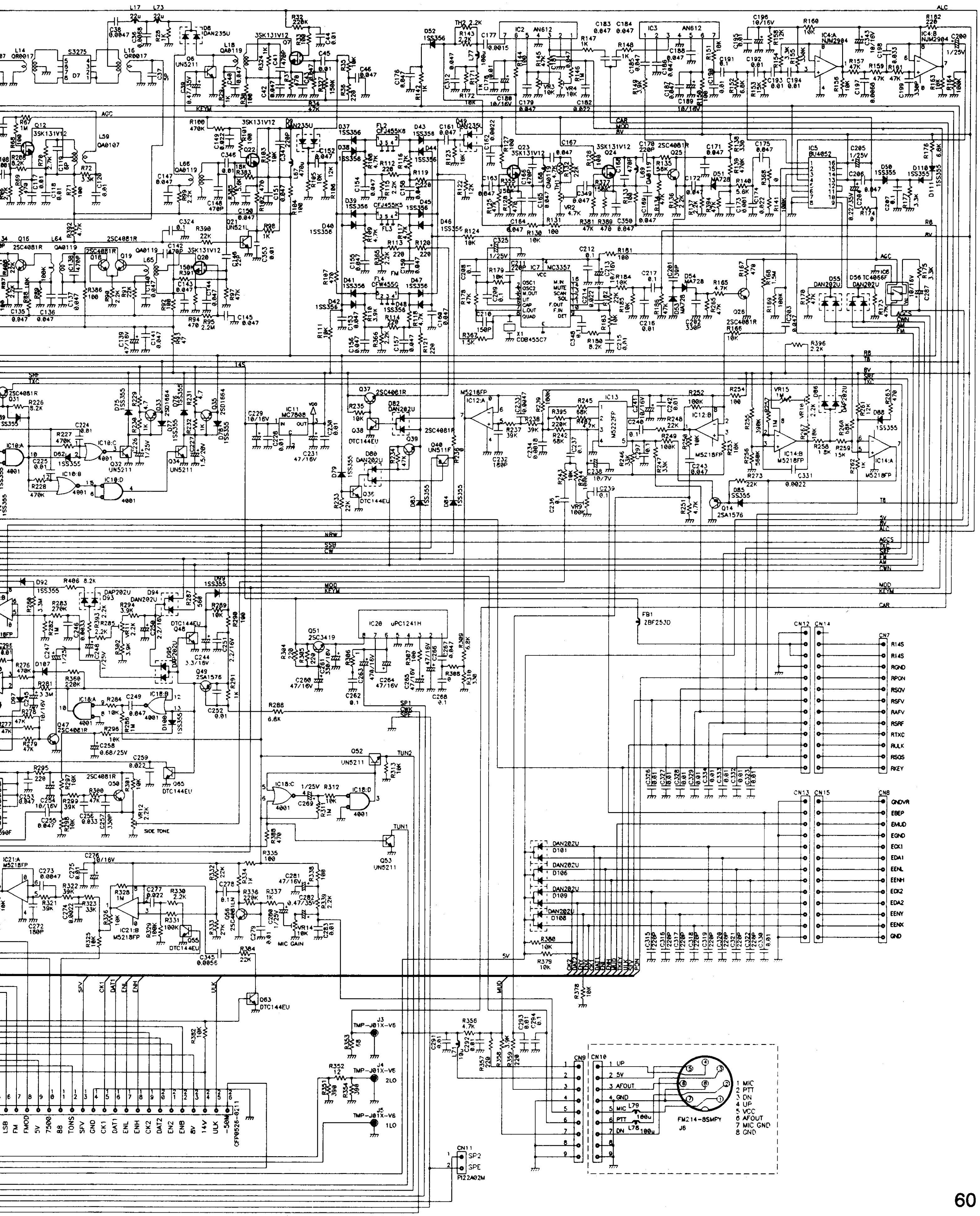


BLOCK DIAGRAM



CIRCUIT DIAGRAM MAIN UNIT

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R14S
RGND
RPON
RSOV
RSFV
RAFV
RSRF
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RULK
RSOS
RKEY
CN8
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EBEP
EMUD
EGND
ECK1
EDA1
EENL
EENH
ECK2
EDA2
EENY
EENX
GND
CN11
SP2
SPE
PI22A02M
1 MIC
2 PTT
3 DN
4 UP
5 VCC
6 AFOUT
7 MIC GND
8 GND
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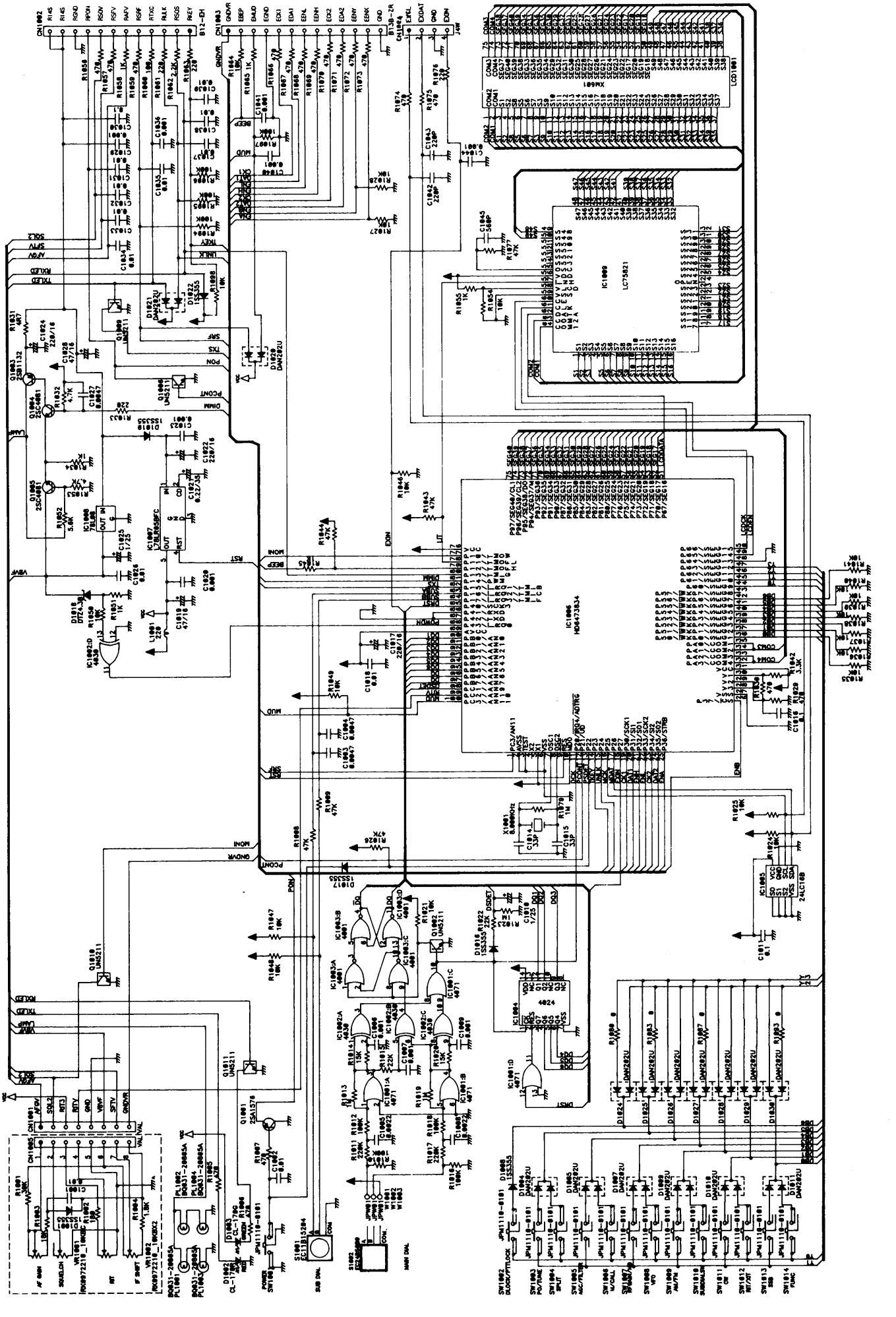
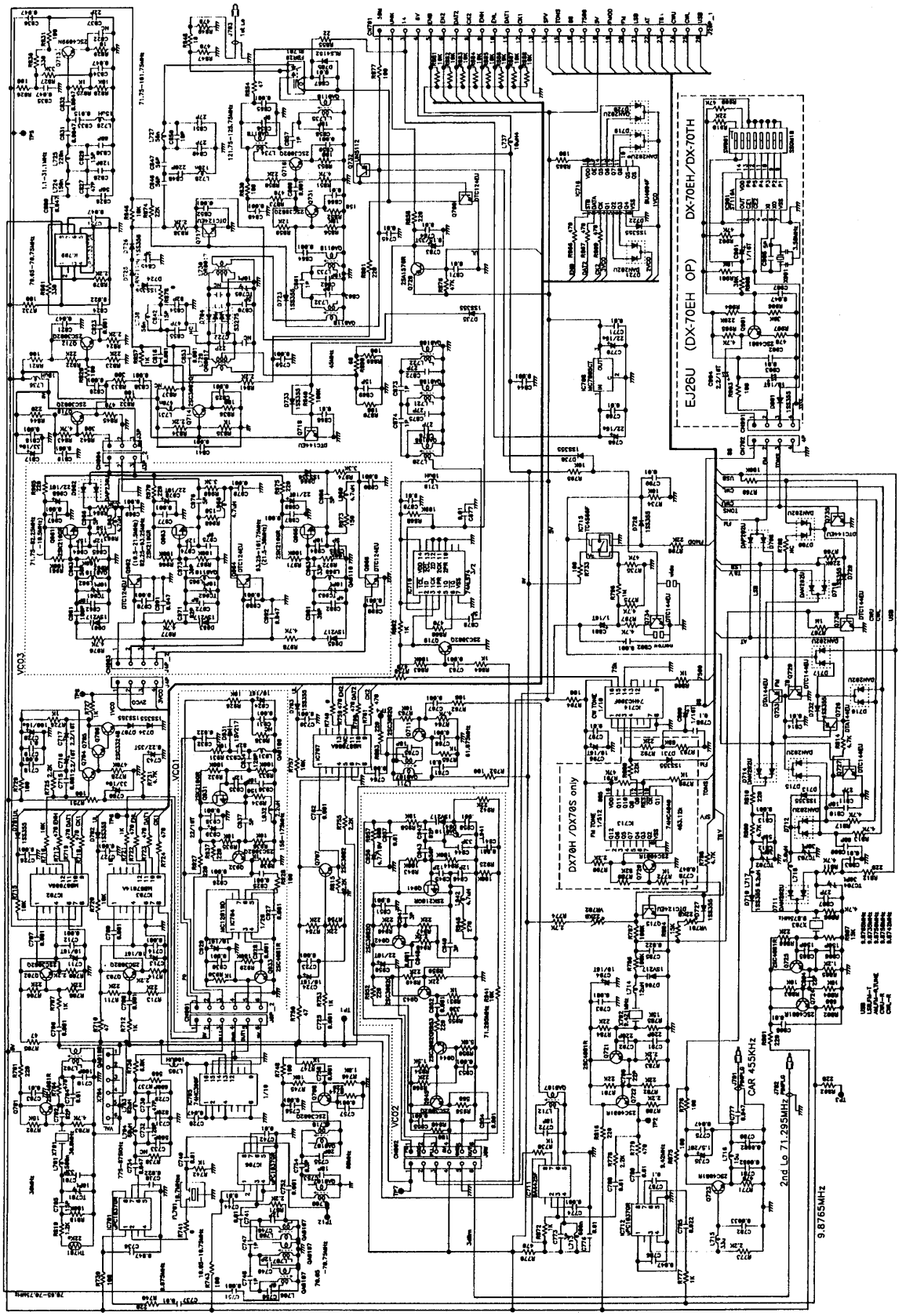
MIC GAIN
SIDE TONE
TMP-J01X-V6
CFP0526-0211



PLL UNIT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DX-70EH/DX-70TH
DX70H /DX70S only
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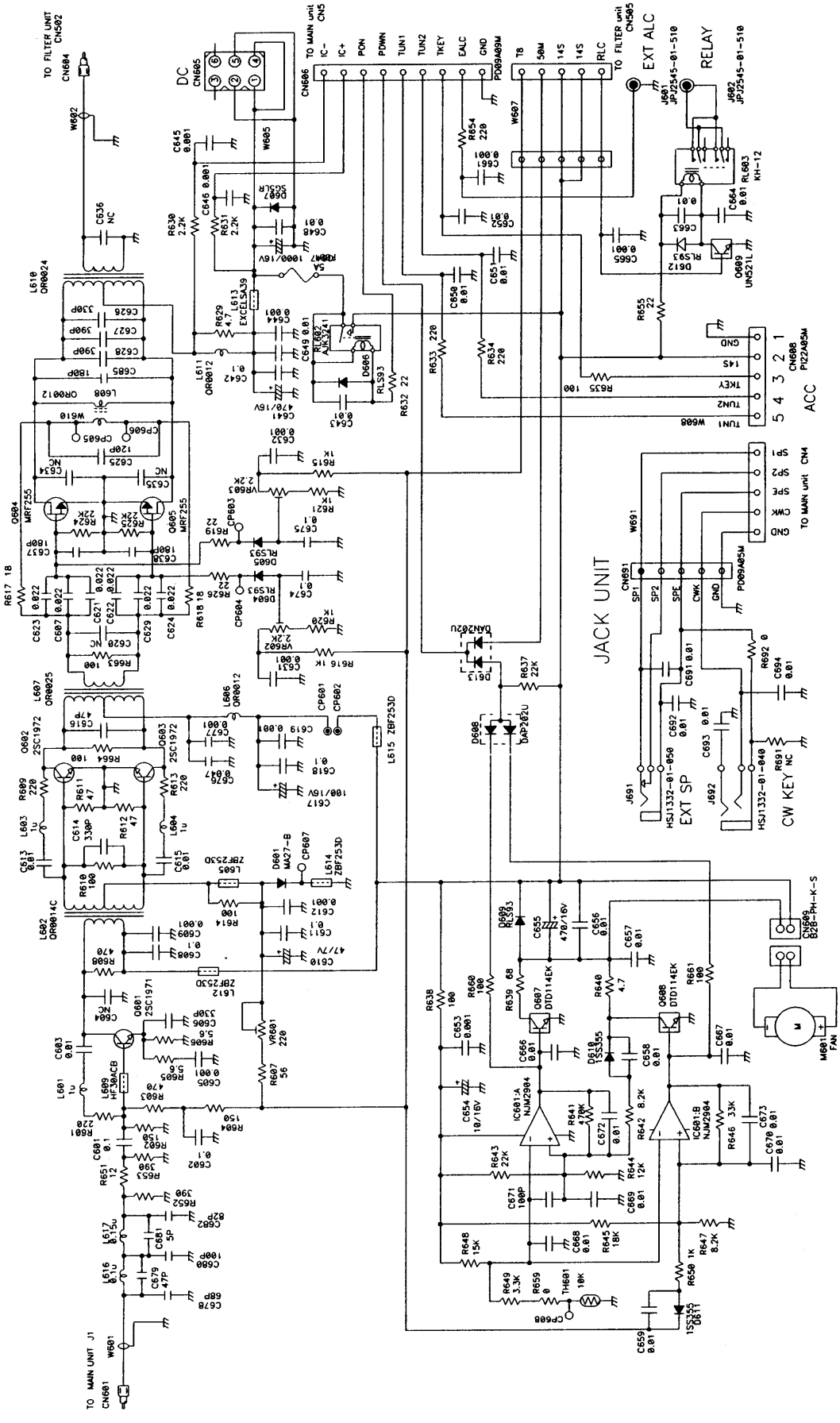
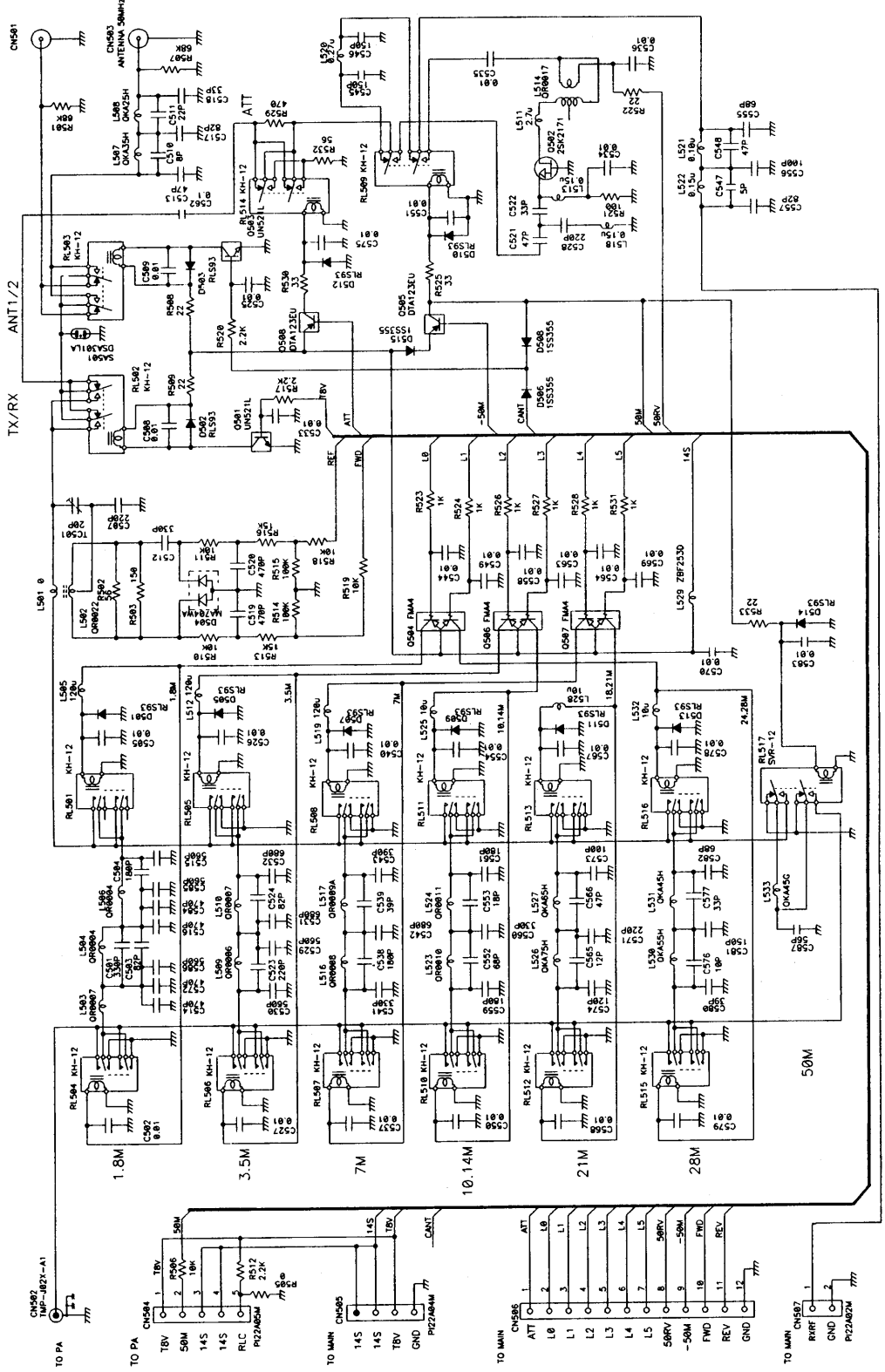
VCO2
VCO3
CAR 455KHz
2nd Lo 71.295MHz
9.8765MHz

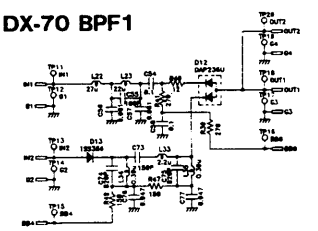
PA UNIT


JACK UNIT
EXT SP
CW KEY
ACC
RELAY
EXT ALC
DC
FAN
TO MAIN UNIT J1
TO FILTER UNIT CN502
TO MAIN unit CN5
TO FILTER unit CN505
TO MAIN unit CN4

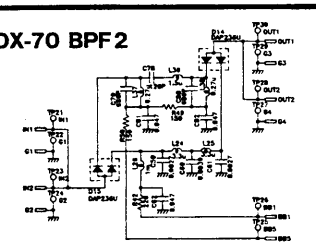
FILTER UNIT



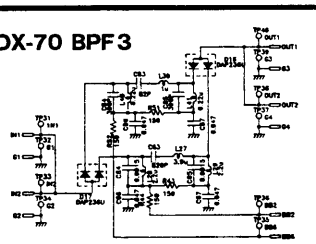
DX-70 BPF1



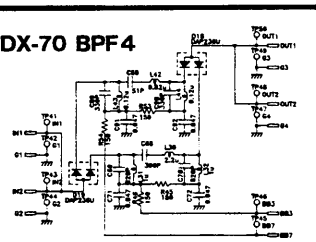
DX-70 BPF2



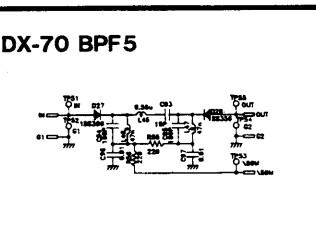
DX-70 BPF3



DX-70 BPF4

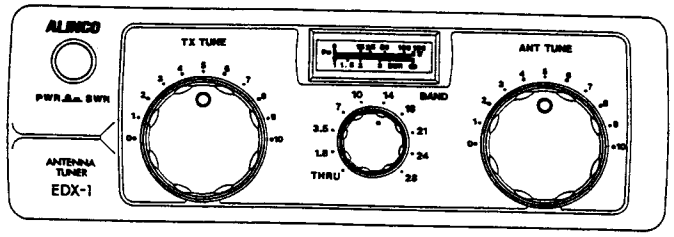


DX-70 BPF5

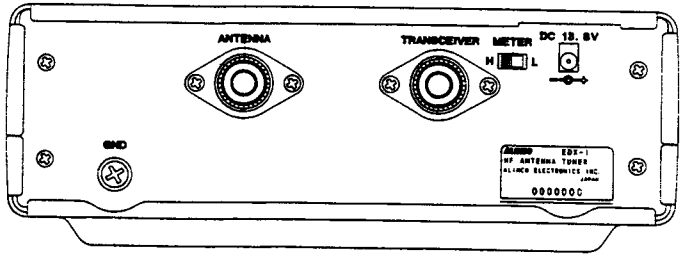


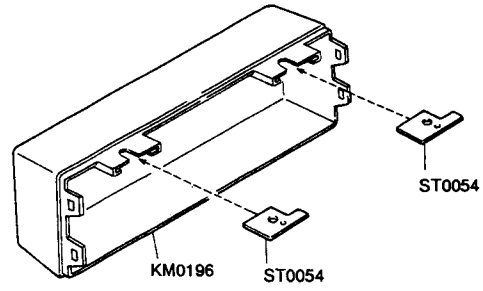
Exploded View for EDX-1

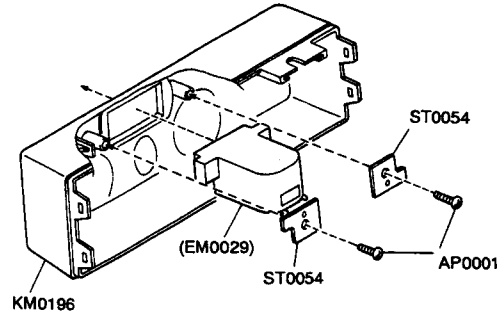
1) Front View

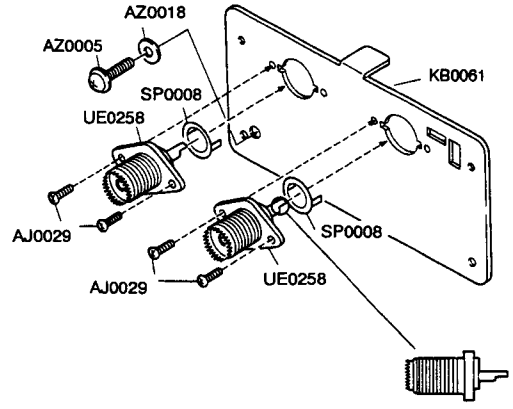


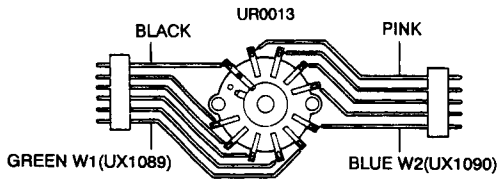
2) Rear View

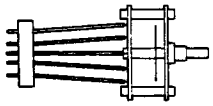


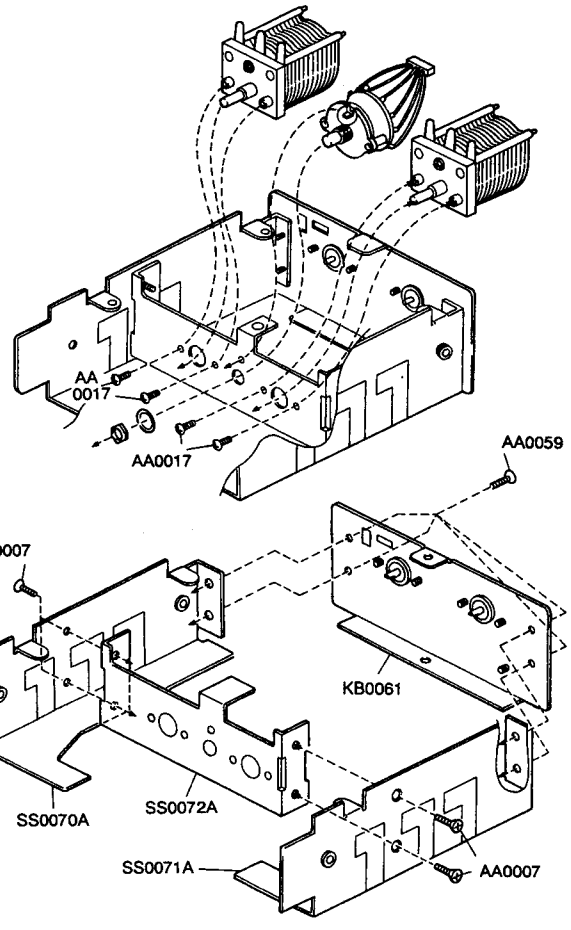







UR0013
BLACK
PINK
GREEN W1(UX1089)
BLUE W2(UX1090)

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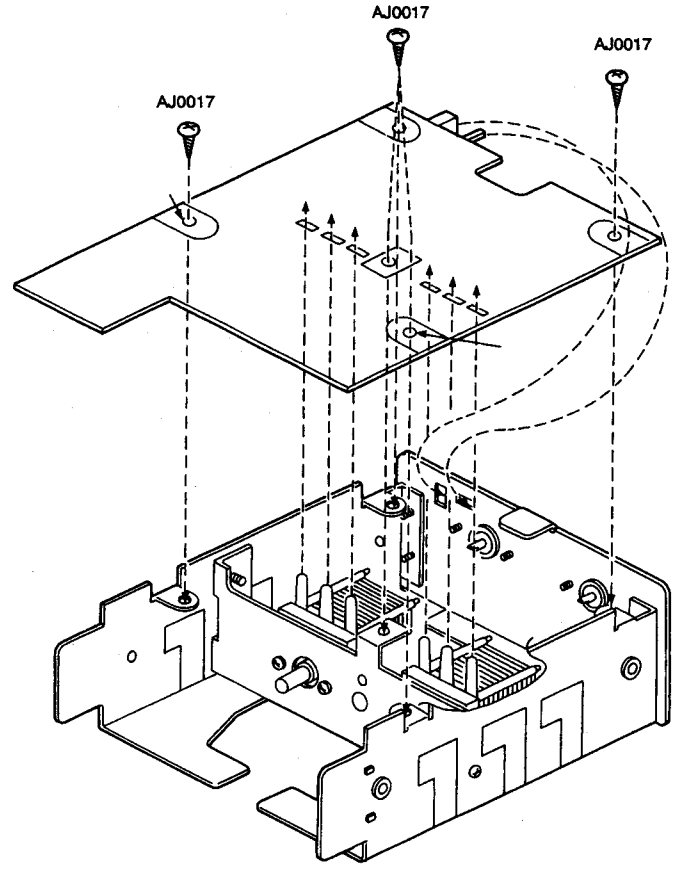
0017
AA0017
AA0059
AA0007
KB0061
SS0070A
SS0072A
SS0071A
AA0007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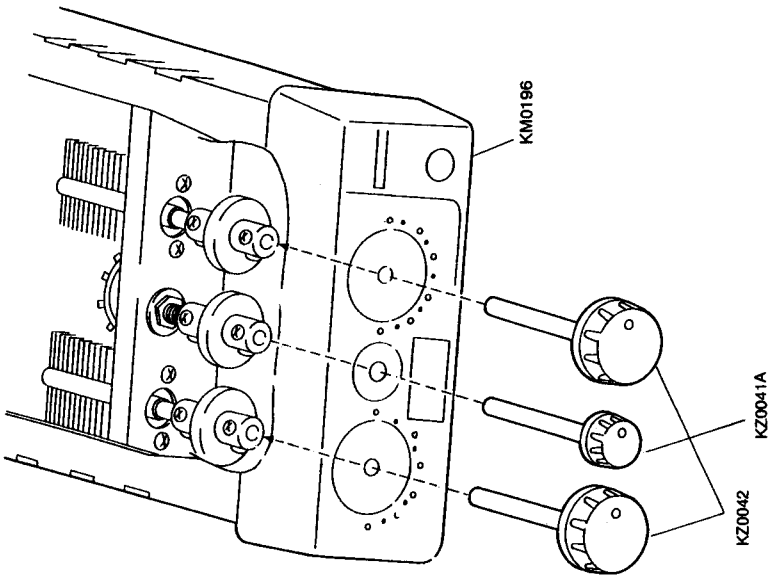
AJ0017
AJ0017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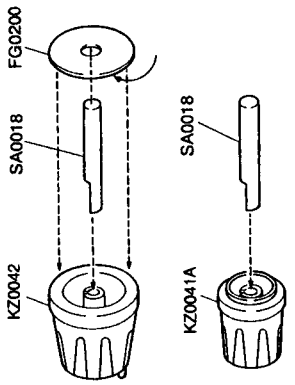
KZ0041A
KZ0042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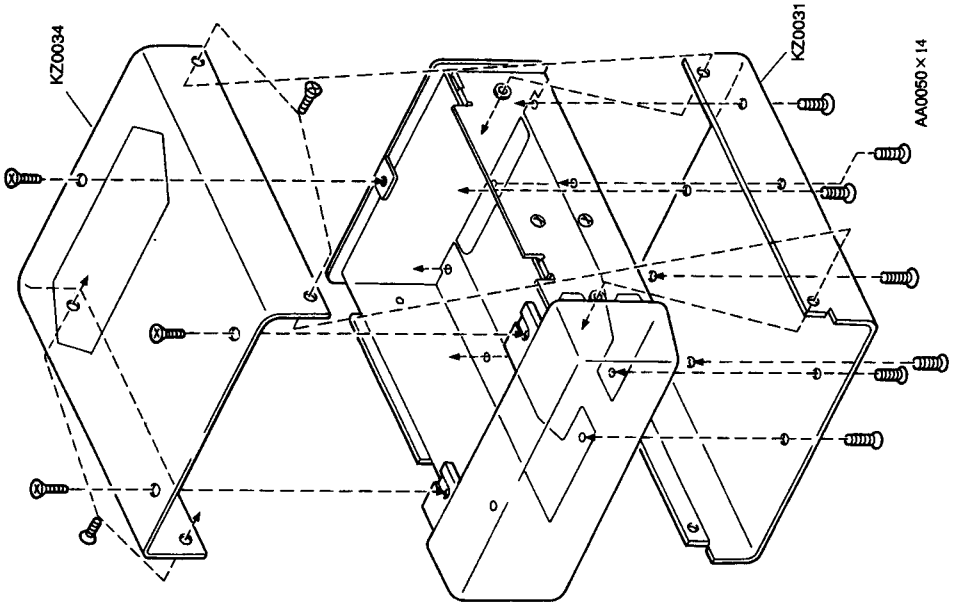
SA0018
KZ0042
SA0018
KZ0041A


KZ0034
KZ0031
AA0050×14

Parts List for EDX-1

Ref. No.	Parts No.	Parts Name	Loc
		Tuner	
C1	CU3047	C1608JB1H103KT-A	A
C2	CE0201	16MV10SZ SEI	M
C3	CE0201	16MV10SZ SEI	M
C4	CU3047	C1608JB1H103KT-A	A
C5	CU3027	C1608CH1H221KT-A	A
C6	CU3029	C1608JB1H331KT-A	A
C7	CU3031	C1608JB1H471KT-A	A
C8	CU3031	C1608JB1H471KT-A	A
C9	CU3101	C1608JB1C473KT-A	A
C10	CU3101	C1608JB1C473KT-A	A
C11	CU3101	C1608JB1C473KT-A	A
C12	CU3031	C1608JB1H471KT-A	A
C13	CU3044	C1608JB1H562KT-A	A
C14	CS0060	TMCSA1E474MTR	A
C15	CU3047	C1608JB1H103KT-A	A
C16	CU3047	C1608JB1H103KT-A	A
C17	CU3047	C1608JB1H103KT-A	A
C18	CU3047	C1608JB1H103KT-A	A
C19	CU3047	C1608JB1H103KT-A	A
C20	CU3047	C1608JB1H103KT-A	A
C21		NC NC	
C22	CU3047	C1608JB1H103KT-A	A
C23	CU3047	C1608JB1H103KT-A	A
C24	CU3047	C1608JB1H103KT-A	A
C25	CU3047	C1608JB1H103KT-A	A
C26	CU3047	C1608JB1H103KT-A	A
C27	CU3047	C1608JB1H103KT-A	A
C28	CU3030	C1608JB1H391KT-A	A
C29	CU3047	C1608JB1H103KT-A	A
C30	CU3047	C1608JB1H103KT-A	A
D1	XD0273	RLS-93 TE11	A
D2	XD0297	MA8100 TX	A
D3	XD0127	MA704WA TX	A
D4	XD0273	RLS-93 TE11	A
D5	XD0273	RLS-93 TE11	A
IC1	XA0224	NJM2904M-T1 JRC	A
IC2	XA0224	NJM2904M-T1 JRC	A
J1	UJ0033	HEC2781-010520	M
JP1	RD1013	JPW02 R01	H
JP2	RD1013	JPW02 R01	H
JP3	RD1013	JPW02 R01	H
JP4	RD1013	JPW02 R01	H
JP5	RD1013	JPW02 R01	H
JP6	RD1013	JPW02 R01	H
JP7	RD1013	JPW02 R01	H
JP8	RD1013	JPW02 R01	H
JP9	RD1013	JPW02 R01	H
JP10		NC NC	
JP11	RK1107	ERJ8GEY0R00V	A
L1	RD1013	JPW02 R01	H
L2	QR0013A	Toroidal Coil QR0013A	H
L3	QKB002	COIL QKB002	H
L4	QR0019	Toroidal Coil QR0019	H
L5	QR0020	Toroidal Coil QR0020	H
L6	QC0048	NL322522T-100J	A
Q1	XT0113	2SC2873Y TE12L	A
Q2	XU0148	DTC144EU T106	A
Q3	XU0148	DTC144EU T106	A
R1	RK4087	ERJ14YJ151V	A
R2	RD0001	ERD S2TJ 100	M
R3	RK4029	ERJ-12YJ181H	A
R4	RK4024	ERJ-12YJ680H	A
R5	RK3050	ERJ3GSYJ103V	A
R6	RK3050	ERJ3GSYJ103V	A
R7	RK3052	ERJ3GSYJ153V	A
R8	RK3052	ERJ3GSYJ153V	A
R9	RK3060	ERJ3GSYJ683V	A
R10	RK3062	ERJ3GSYJ104V	A
R11	RK3062	ERJ3GSYJ104V	A
R12	RK3062	ERJ3GSYJ104V	A
R13	RK3050	ERJ3GSYJ103V	A
R14	RK3050	ERJ3GSYJ103V	A
R15	RK3063	ERJ3GSYJ124V	A
R16	RK3048	ERJ3GSYJ682V	A
R17	RK3050	ERJ3GSYJ103V	A
R18	RK3054	ERJ3GSYJ223V	A
R19	RK3048	ERJ3GSYJ682V	A
R20	RK3050	ERJ3GSYJ103V	A
R21	RK3050	ERJ3GSYJ103V	A
R22	RK3057	ERJ3GSYJ393V	A
R23	RK3074	ERJ3GSYJ105V	A
R24	RK3057	ERJ3GSYJ393V	A
R25	RK3057	ERJ3GSYJ393V	A
R26	RK3062	ERJ3GSYJ104V	A
R27	RK3050	ERJ3GSYJ103V	A
R28	RK0001	ERJ6GEYJ100V	A
R29	RK3026	ERJ3GSYJ101V	A
R30	RK3070	ERJ3GSYJ474V	A
R31	RK3026	ERJ3GSYJ101V	A
RL1	UL0015	SVR-12	M
RL2	UL0015	SVR-12	M
SW1	UQ0015	SPPJ22727A	M
SW2	UR0013	SRRY101AN-R15	H
SW3	US0020	ESD1522209	M
TC1	CT0036	ECV1ZW20X64T	M
VC1	CV0001	UV44B 300P	H
VC2	CV0001	UV44B 300P	H
VR1	RH0105	EVM1YSX50BY4	A
VR2	RH0106	EVM1YSX50BQ4	A
W1	UX1089	Wires EDX-1 1	H
W2	UX1090	Wires EDX-1 2	H
W3	UX1091	Wires EDX-1 3	H
W4	UX1091	Wires EDX-1 3	H
	UP0291	EDX-1 PC Board	T

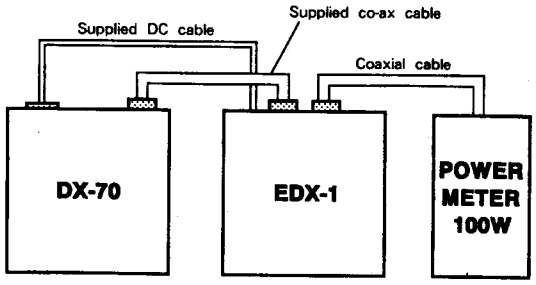
Packing

Parts No.	Parts Name
HK0386A	PACKAGE EDX-1
HP0009	Protect. Bag (5×125×250)
HP00039	Protect. Bag (65×250×400)
HU0080	P.MTL/CARTON(A)DX70
HU0082	P.MTL/CARTON(A)DX70
HU0087	P.MTL/CARTON(A)DX70
PS0229	INSTRUCTION MANUAL EDX1
PT0004A	SERIAL NO. FOR CARTON
UA0049	EDX1 DC CODE
UE0264	M-M CABLE EDX1

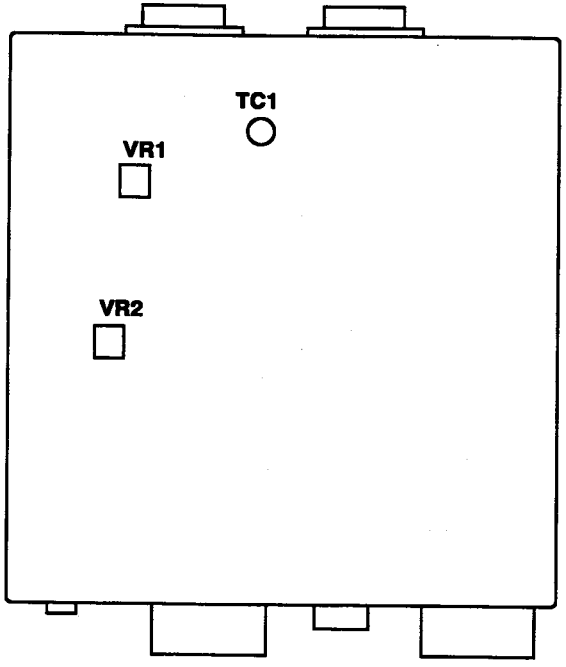
Mechanical Parts

Parts No.	Parts Name
PR0288	LABEL(SCREW STKR DX-70)
DS03898A	Serial No. PLATE(NEW)
AA0007	SCREW FH M2.6+6 Fe/Zn
AA0017	SCREW PH M3+8 Fe/Zn
AA50	SCREW OH M2.6+6 Fe/B.Zn
AA0059	SCREW BH M2.6+6 Fe/Ni
AD0005	SCREW PH/D M4+10 Fe/Zn
AJ0017	SCREW TH T2.6+6 Fe/N
AJ0029	SCREW PH T3+6 Fe/Zn
AP0001	SCREW PH M2.6+8 Fe/Zn
AZ0018	WASHER PW 4×10×0.8 Fe/Zn
EM0029	METER KL284A55
FG0200	DIAL PAT
KB0061	REAR CASE
KM0196	FRONTCASE
KZ0031	BOTTOM COVER DX-70
KZ0034	UPPERCASE EDX-1
KZ0041A	SUBDIAL EDX-1
KZ0042	DIAL DX-701
NS0005	SW KNOB(PS) CIRCLE
PR0292	LABEL (KNOB)
SA0018	STAY D6×60
SP0008	TERMINAL(GND DX-70)
SS0070A	CHASSIS(LEFT)
SS0071A	CHASSIS(RIGHT)
SS0072A	CHASSIS(CENTER)
ST0054	FIX METER
TZ0065	CUP RING C
UE0258	FM-M.D.R-(4)
UR0013	CONNECTOR SRRY101AN-R15
UX1089	WIRE EDX-1 W1
UX1090	WIRE EDX-1 W2

Connection Example



Adjustment Point



Required Test Equipment for EDX-1

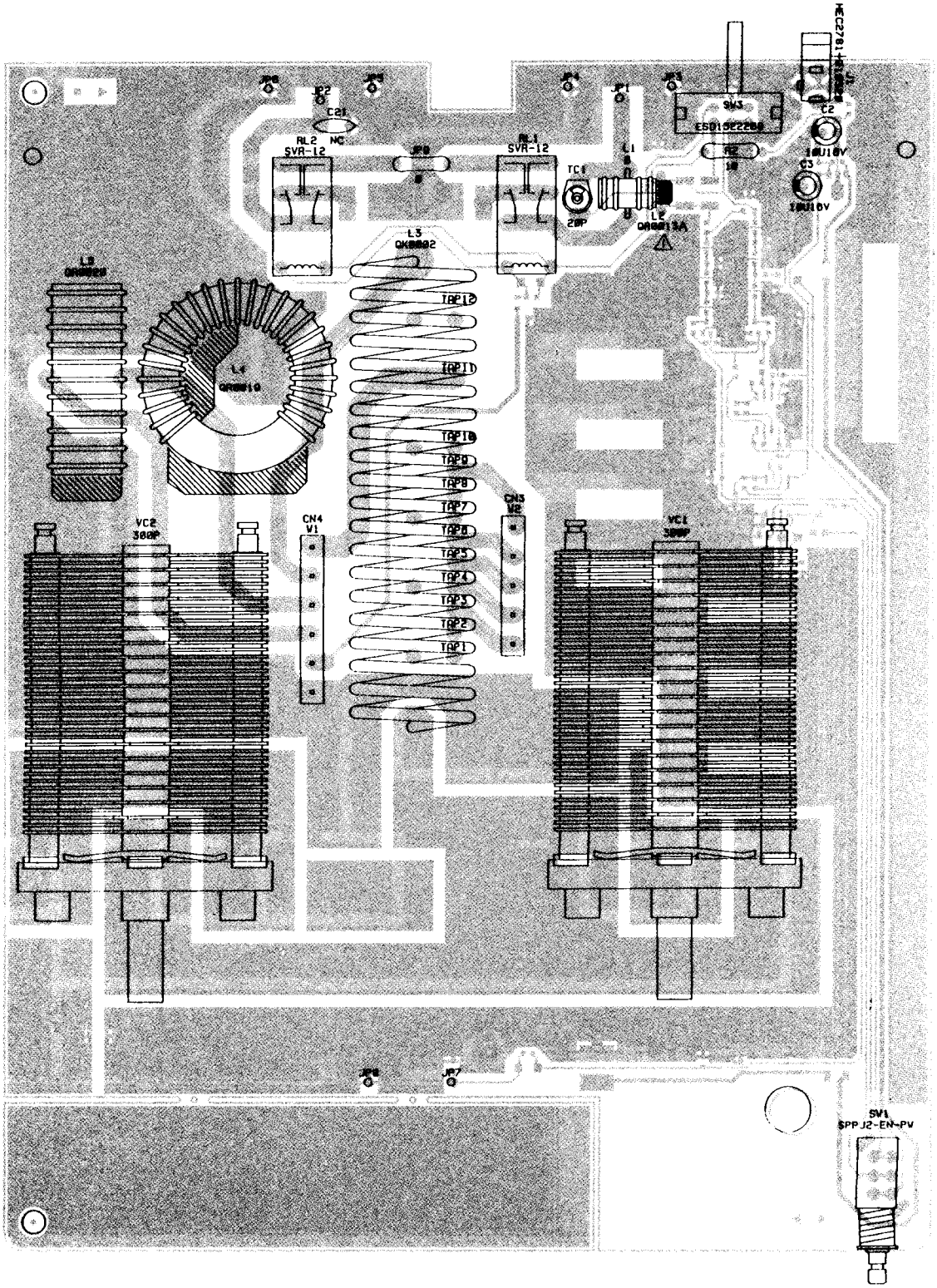
TX ON	BAND	SWR	METER	TX TUNE	ANT TUNE	METER READING	UNIT
14.1MHz 100W	1.8	ON	H	10	10	∞	SWR
14.1MHz 100W	THRU	OFF	H	–	–	100W	PWR
14.1MHz 10W	THRU	OFF	L	–	–	10W (100W on scale)	PWR
1.9MHz 100W	1.8	ON	H	4	4	1.5max.	SWR
3.6MHz 100W	3.5	ON	H	7	7	1.5max.	SWR
7.1MHz 100W	7	ON	H	6	6	1.5max.	SWR
10.1MHz 100W	10	ON	H	7.5	7.5	1.5max.	SWR
14.1MHz 100W	14	ON	H	8	8	1.5max.	SWR
18.1MHz 100W	18	ON	H	8.5	8.5	1.5max.	SWR
21.1MHz 100W	21	ON	H	9	9	1.5max.	SWR
24.9MHz 100W	24	ON	H	9	9	1.5max.	SWR
28.1MHz 100W	28	ON	H	9	9	1.5max.	SWR

Adjustment for EDX-1

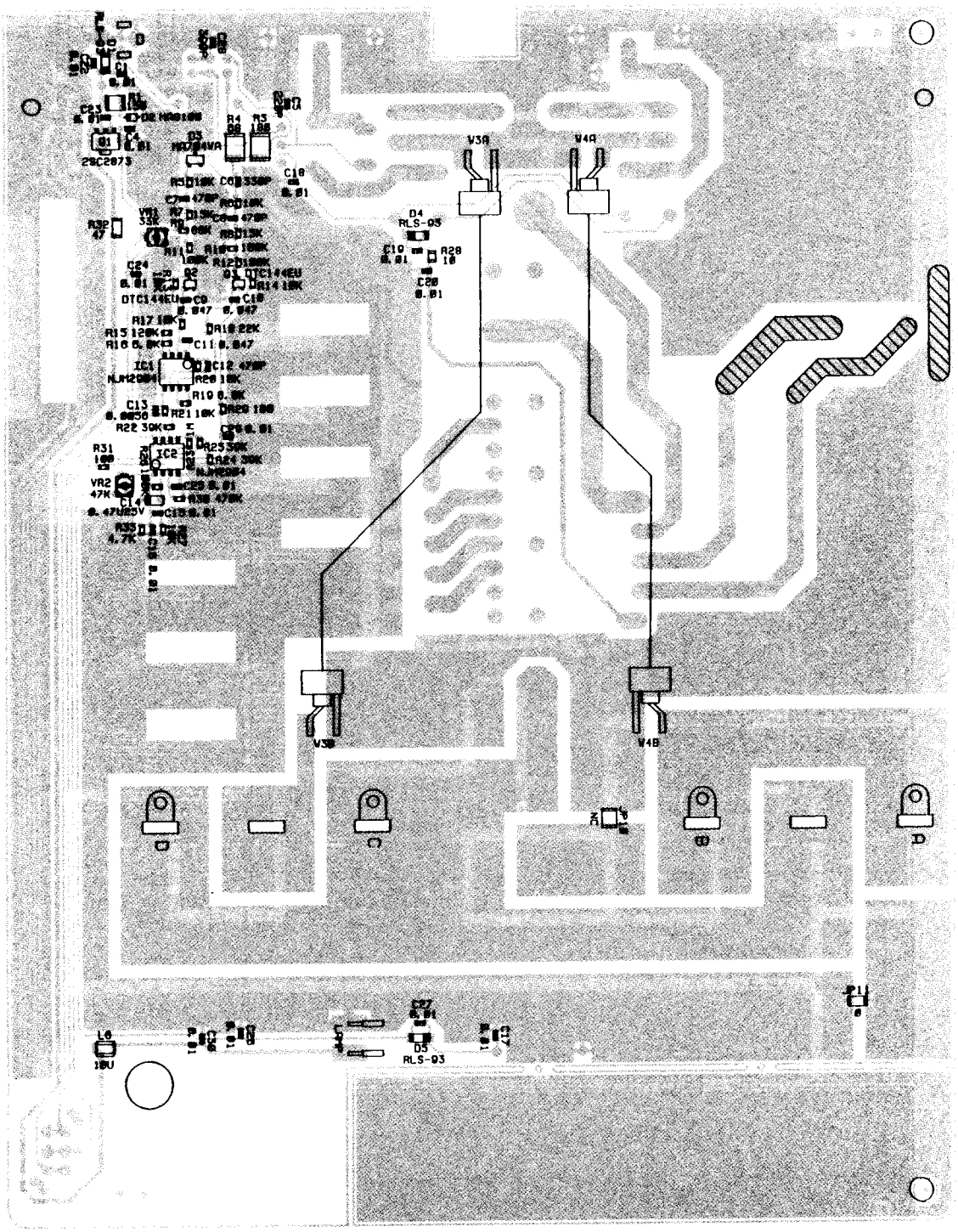
DX-70 TX FREQ. 14.1MHz TX POWER 100W						
BAND	SWR	METER	TX TUNE	ANT TUNE	ADJUST POINT	METER READING
THRU	ON	H	–	–	TC 1	MIN
1.8	ON	H	10	10	VR 2	∞
THRU	OFF	H	–	–	VR1	100W

PC Bord View for EDX-1

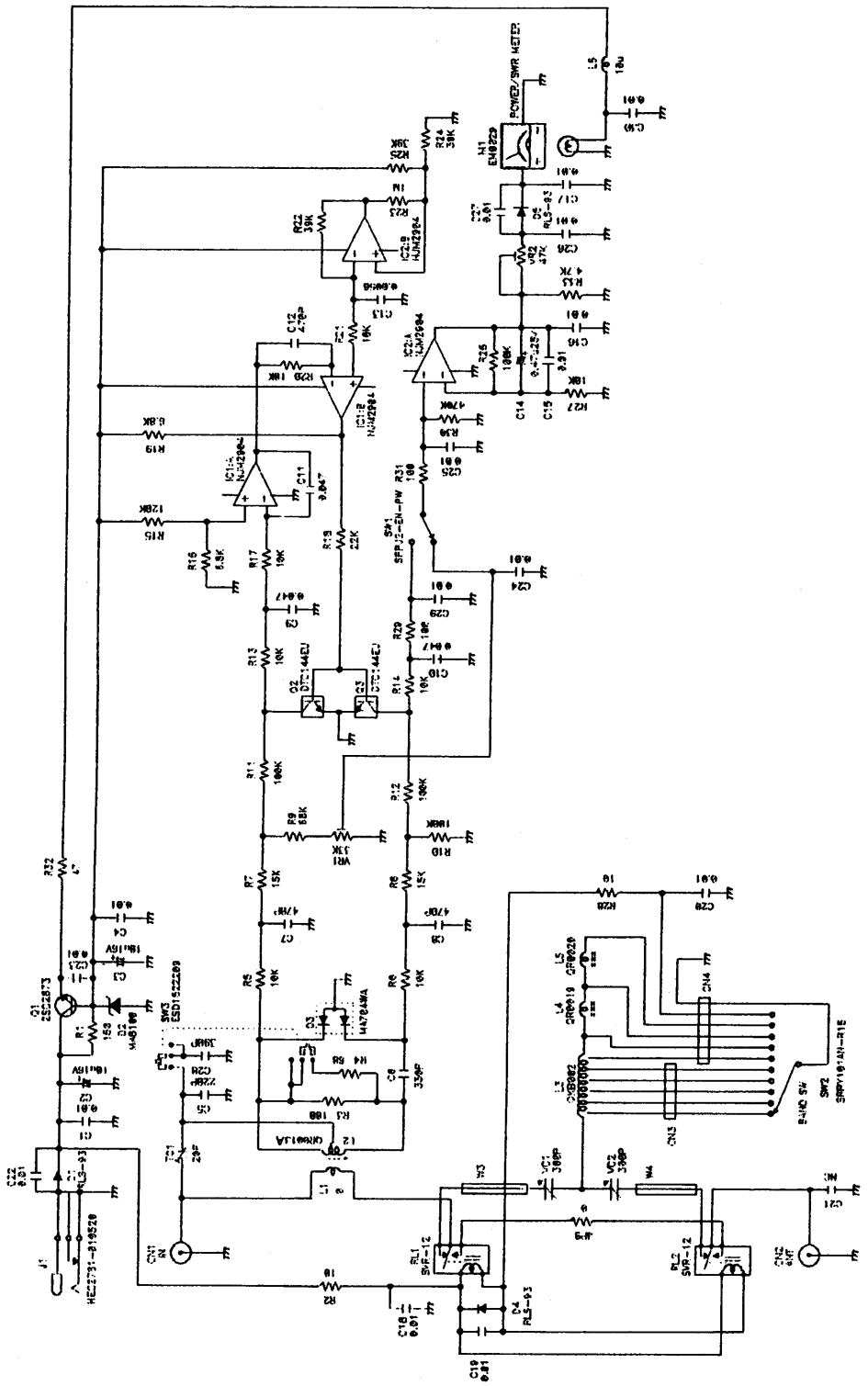
Side A

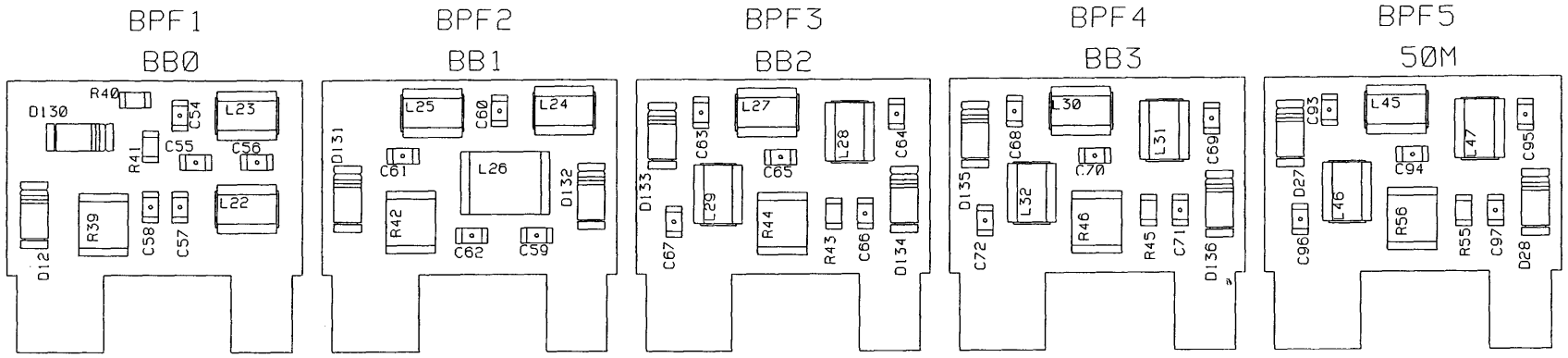


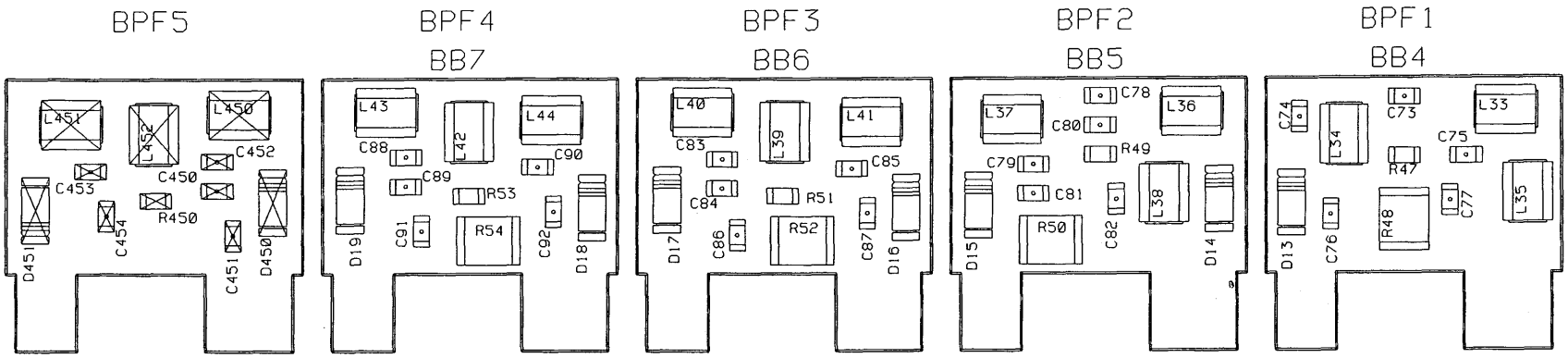
Side B



Schematic Diagram for EDX-1




BPF1
BB0
R40
D130
C54
L23
C55
C56
R41
L22
R39
C58
C57
D12
BPF2
BB1
L25
C60
L24
D131
C61
L26
D132
R42
C62
C59
BPF3
BB2
D133
C63
L27
L28
C64
C65
L29
R44
R43
C66
C67
D134
BPF4
BB3
D135
C68
L30
L31
C69
C70
L32
R46
R45
C71
C72
D136
BPF5
50M
C93
L45
L47
C95
C94
D27
L46
R56
R55
C97
C96
D28


BPF5
BPF4
BB7
BPF3
BB6
BPF2
BB5
BPF1
BB4
L451
L452
L450
C452
C450
C453
C454
R450
D451
C451
D450
L43
C88
L42
L44
C90
C89
R53
D19
C91
R54
C92
D18
L40
C83
L39
L41
C85
C84
R51
D17
C86
R52
C87
D16
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L38
D15
R50
C82
D14
C74
L34
C73
L33
C75
R47
C77
L35
D13
C76
R48